G-Link connection test
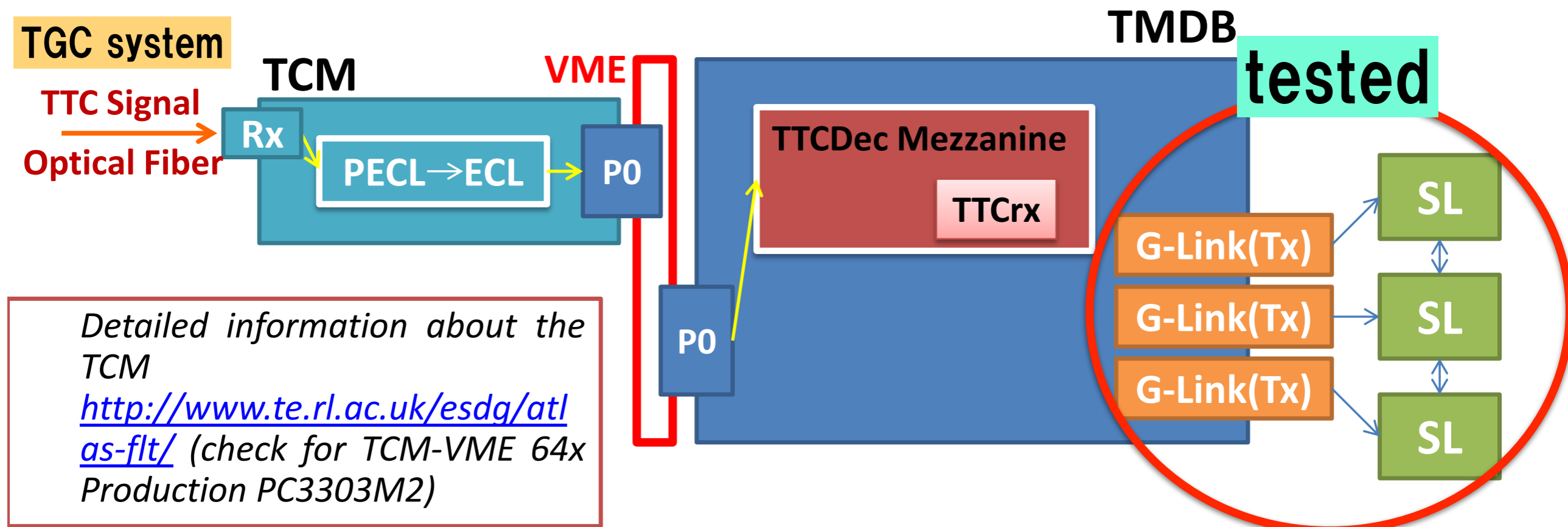## between TGC SectorLogic and TMDB
in blg. 175

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TileMuon Meeting

Overview

TGC system

TTC Signal
Optical Fiber

TCM

VME

Rx → PECL→ECL → P0

TMDB

tested

TTCDec Mezzanine

TTCrx

P0

G-Link(Tx) → SL

G-Link(Tx) → SL

G-Link(Tx) → SL

SL

Detailed information about the TCM http://www.te.rl.ac.uk/esdg/atlas-flt/ (check for TCM-VME 64x Production PC3303M2)
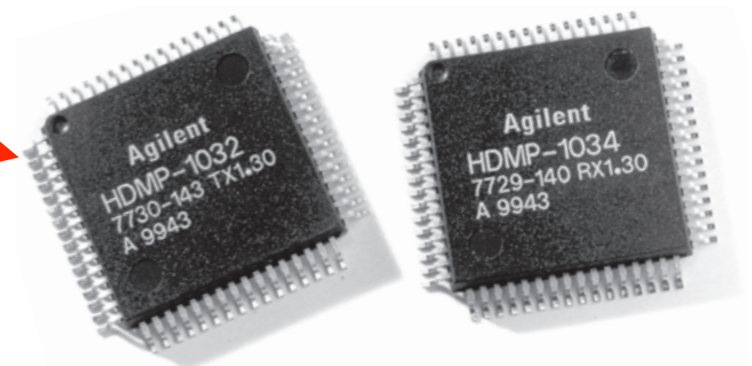
There is no G-Link Transmitter Chip on TMDB, and data is sent via FPGA. Since this is the first time to receive data sent by such a scheme, we checked the connection carefully.

items to check
1. readout data

a) dumped in a general-purpose module (PT5)

b) readout in SL

2. link recovery

G-Link Transmitter/ Receiver Chip

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1.a) dumped in a general-purpose module

We dumped the G-Link signal from TMDB.

G-Link status bits

sd	rxready	rxerror	rxdslip
1	1	0	0

sd   = 1 : signal is detected
rxready = 1 : there is no error
rxerror = 0 : data/control/idle word is received
rxdslip = 0 : TX's clock is same with RX's clock

rxcntl	rxdata
0	1

rxcntl = 0, rxdata = 1
we sent data words

Datawords are sent without error

G-Link data bits

patterns to check	readout (binary)
0	0000 0000 0000 0000
1st. bit	0000 0000 0000 0001
2nd. bit	0000 0000 0000 0010
3rd. bit	0000 0000 0000 0100
4th. bit	0000 0000 0000 1000
…	…
16th. bit	1000 0000 0000 0000
0	0000 0000 0000 0000

all bits are checked

We can read the G-Link signal from TMDB correctly

We checked consistency of data patterns which are sent from TMDB and readout in SL
(input format has 16bits, output format has 8bits)

	Module3				Module2				Module1				Module0			
	D5+D6		D6		D5+D6		D6		D5+D6		D6		D5+D6		D6	
	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L
input pattern	0	0	0	0	0	1	0	0	0	0	1	0	0	1	1	0
	D5+D6		D6		D5+D6		D6		D5+D6		D6		D5+D6		D6	
converted pattern	0		0		1		0		0		1		1		1	
output pattern	0		0		1		0		0		1		1		1	

The patterns are precisely matched with the input patterns

We can correctly receive the G-Link signal from TMDB in SL

2. link recovery

G-Link connection would be lost when the LHC clock is changed. We need to check if the G-Link connection will be correctly recovered when the clock is back.

40.08 MHz

```
1100_01_0000000000000000
1100_01_0000000000000000
1100_01_0000000000000000
1100_01_0000000000000000
1100_01_0000000000000000
1100_01_0000000000000000
1100_01_0000000000000000
1100_01_0000000000000000
1100_01_0000000000000000
1100_01_0000000000000000
```

15.00 MHz

```
1010_01_1111111000000000
1010_01_1111111111111100
1010_01_1111111111111100
1010_01_1111111111000100
1010_01_1111111111000100
1010_01_1100000000000000
1010_01_1111111111111111
1010_01_1111111111111111
1010_01_1111111111000011
1010_01_1111111111100000
```

wrong

40.08 MHz

```
1100_01_0000000000000000
1100_01_0000000000000000
1100_01_0000000000000000
1100_01_0000000000000000
1100_01_0000000000000000
1100_01_0000000000000000
1100_01_0000000000000000
1100_01_0000000000000000
1100_01_0000000000000000
1100_01_0000000000000000
```

We checked the G-Link connection recovery

Summary

- We tested the G-Link connection between TGC Sector Logic and TMDB

  ✓ We can correctly receive the G-link signal from TMDB in SL

  ✓ We checked the G-Link connection recovery

To do

♣ We should use the same TTC system for TGC and TileCal in future test.