G-Link connection test
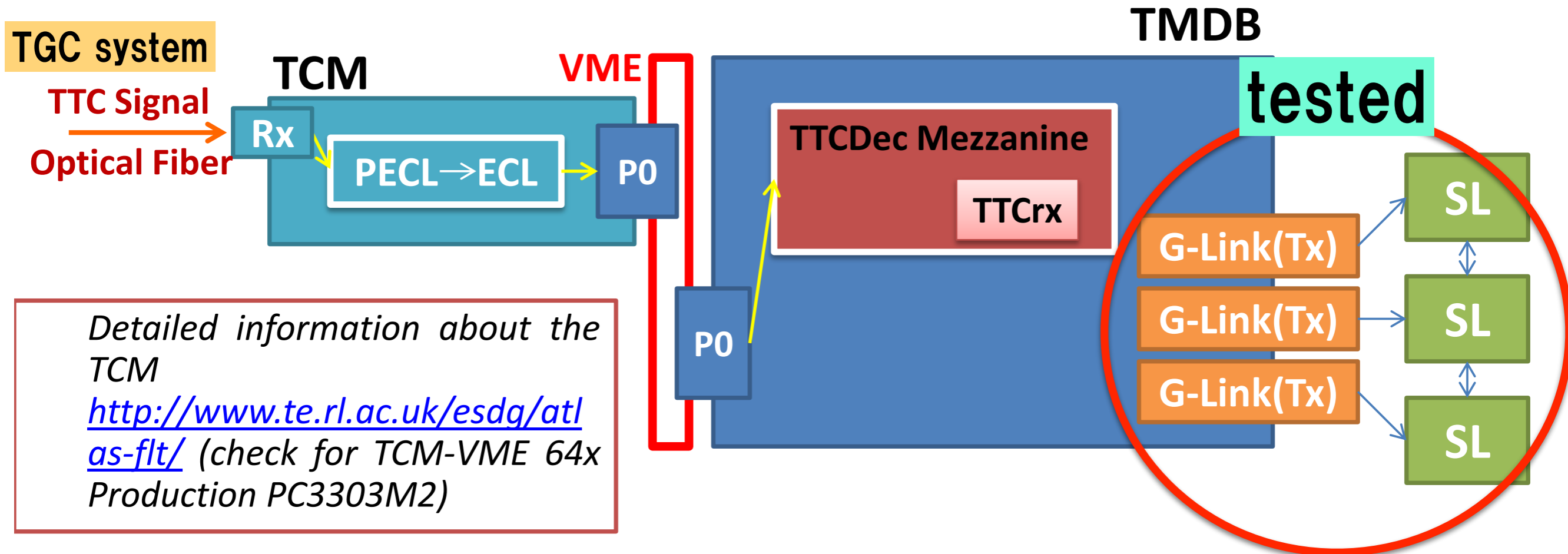## between TGC SectorLogic and TMDB
in bat. 175

Takuto KUNIGO, Makoto HASEGAWA
José Domingos Alves
6/30/ 2014
TileMuon Meeting

Overview

TGC system

TTC Signal

Optical Fiber

TCM

Rx

PECL→ECL

P0

VME

tested

TTCDec Mezzanine

TTCrx

G-Link(Tx)

G-Link(Tx)

G-Link(Tx)

SL

SL

SL

P0

Detailed information about the TCM http://www.te.rl.ac.uk/esdg/atlas-flt/ (check for TCM-VME 64x Production PC3303M2)
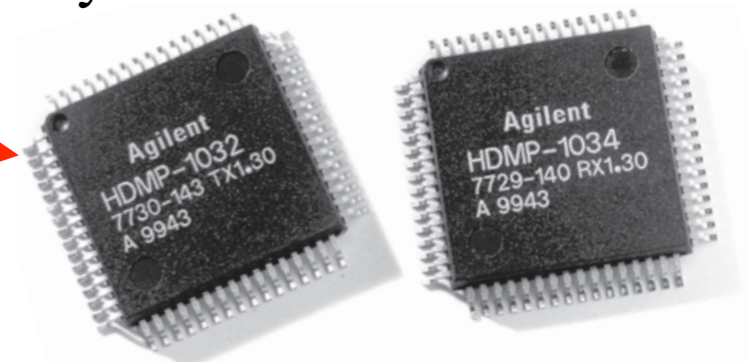
There is no G-Link Transmitter Chip on TMDB, and data is sent via FPGA. Since this is the first time to receive data sent by such a scheme, we checked the connection carefully.

1. readout data
   a) dump module (PT5)

   b) SL

2. link recovery

G-Link Transmitter/ Receiver Chip

1.a) readout data from dump module

We dumped the G-Link signal from TMDB.

G-Link status bits

sd	rxready	rxerror	rxdslip
1	1	0	0

sd   = 1 : signal is detected
rxready = 1 : there is no error
rxerror = 0 : data/control/idle word is received
rxdslip = 0 : TX's clock is same with RX's clock

rxcntl	rxdata
0	1

rxcntl = 0, rxdata = 1
we sent data words

Datawords are sent without error

G-Link data bits

	readout (binary)
0	0000 0000 0000 0000
1st. bit	0000 0000 0000 0001
2nd. bit	0000 0000 0000 0010
3rd. bit	0000 0000 0000 0100
4th. bit	0000 0000 0000 1000
…	…
16th. bit	1000 0000 0000 0000
0	0000 0000 0000 0000

all bits are checked

We can read the G-Link signal from TMDB correctly

1.b) readout data from SL

We used well-known pattern as a SL input,
and checked SL output
(input format has 16bits, output format has 8bits)

	Module3				Module2				Module1				Module0			
	D5+D6		D6		D5+D6		D6		D5+D6		D6		D5+D6		D6	
	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L
input pattern	0	0	0	0	0	1	0	0	0	0	1	0	0	1	1	0

	D5+D6	D6	D5+D6	D6	D5+D6	D6	D5+D6	D6
converted pattern	0	0	1	0	0	1	1	1
output pattern	0	0	1	0	0	1	1	1

The output pattern precisely correspond with the input pattern

SL can receive the G-Link signal from TMDB

2. link recovery

G-Link will be disconnected when LHC clock is changed. It is desirable that G-Link is recovered when clock is recovered.

40.08 MHz

```
1100_01_0000000000000000
1100_01_0000000000000000
1100_01_0000000000000000
1100_01_0000000000000000
1100_01_0000000000000000
1100_01_0000000000000000
1100_01_0000000000000000
1100_01_0000000000000000
1100_01_0000000000000000
1100_01_0000000000000000
```

15.00 MHz

```
1010_01_1111111000000000
1010_01_1111111111111100
1010_01_1111111111111100
1010_01_1111111111000100
1010_01_1111111111000100
1010_01_1111100000000000
1010_01_1111111111111111
1010_01_1111111111111111
1010_01_1111111111000011
1010_01_1111111111100000
```

wrong

40.08 MHz

```
1100_01_0000000000000000
1100_01_0000000000000000
1100_01_0000000000000000
1100_01_0000000000000000
1100_01_0000000000000000
1100_01_0000000000000000
1100_01_0000000000000000
1100_01_0000000000000000
1100_01_0000000000000000
1100_01_0000000000000000
```

G-Link is recovered

Summary

- We tested G-Link connection between TGC Sector Logic and TMDB

  ✓ SL received G-Link signal correctly

  ✓ G-Link is recovered

❖ TGC's TTC system and TileCal's TTC system must be merged for the future test
(Now we are using TGC's TTC only)