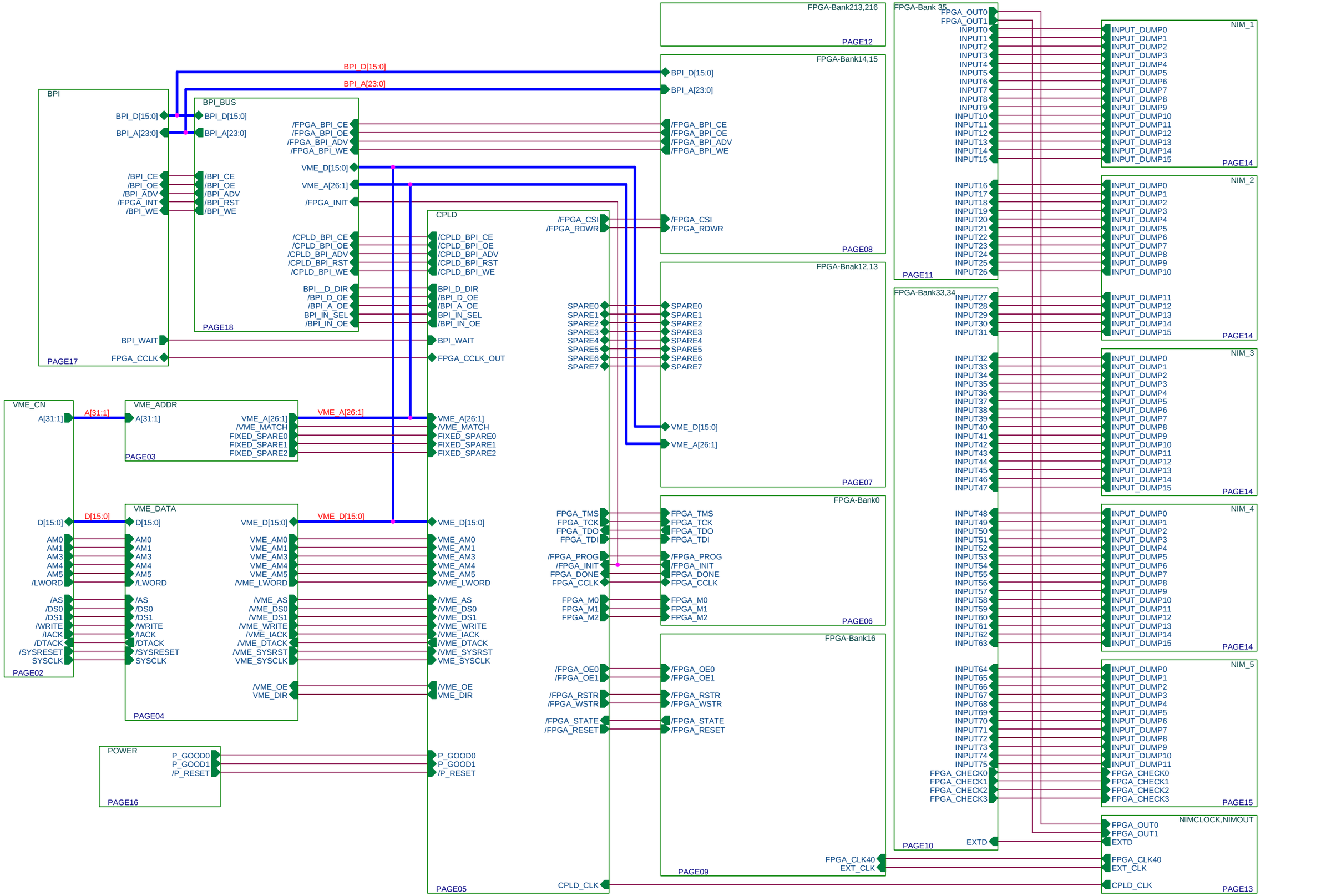
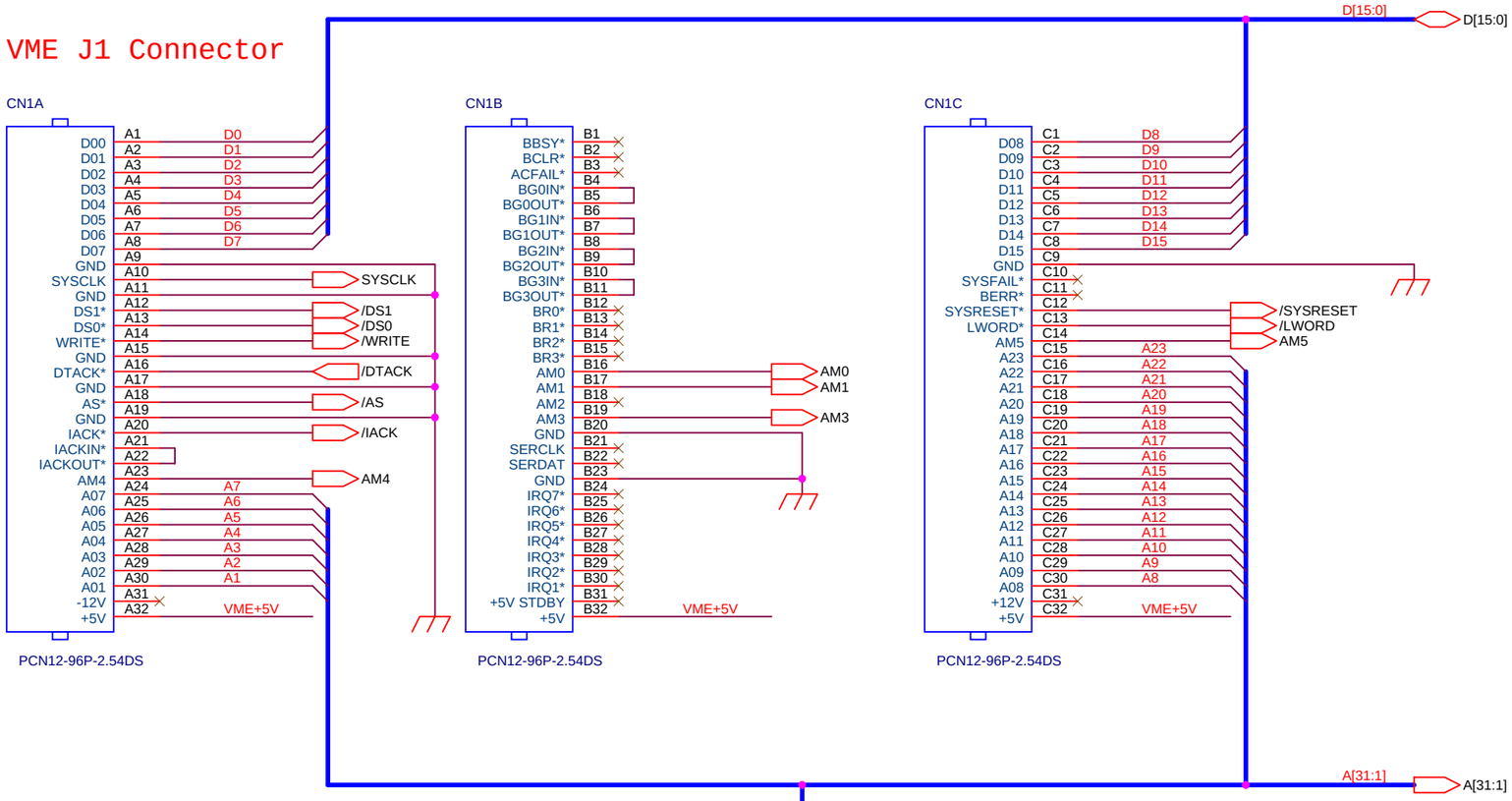


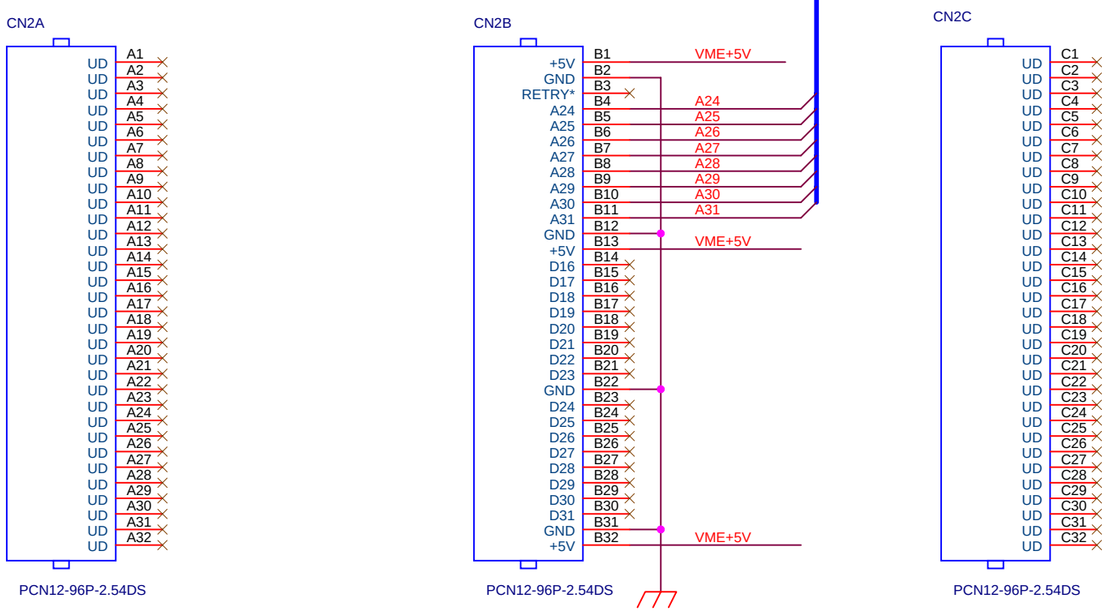
PWB=GN-1457-1

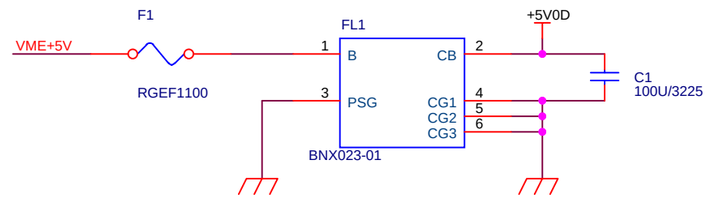
Title	OR_Module for burst stopper	
	TOP	
Size: A3	Document Number: <Doc>	Rev: 3.0
Date: Monday, March 23, 2015	Sheet 1 of 18	

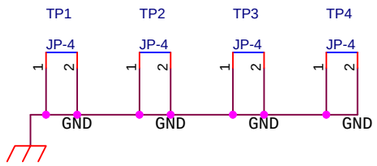
VME J1 Connector



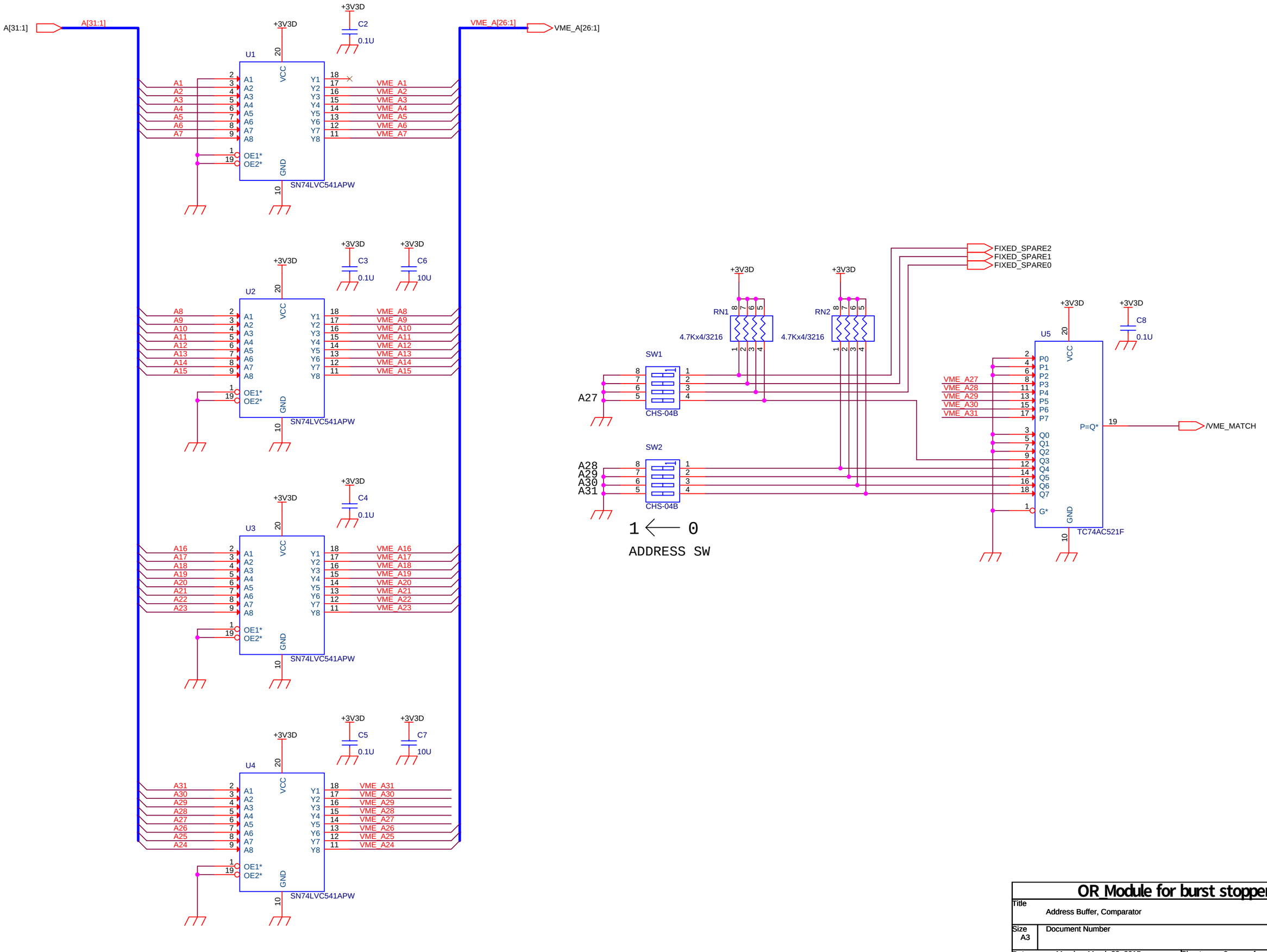
VME J2 Connector







OR_Module for burst stopper			
Title: VME Connector			
Size: A3	Document Number		Rev: 3.0
Date: Monday, March 23, 2015		Sheet 2 of 18	



Title	OR_Module for burst stopper
	Address Buffer, Comparator
Size A3	Document Number
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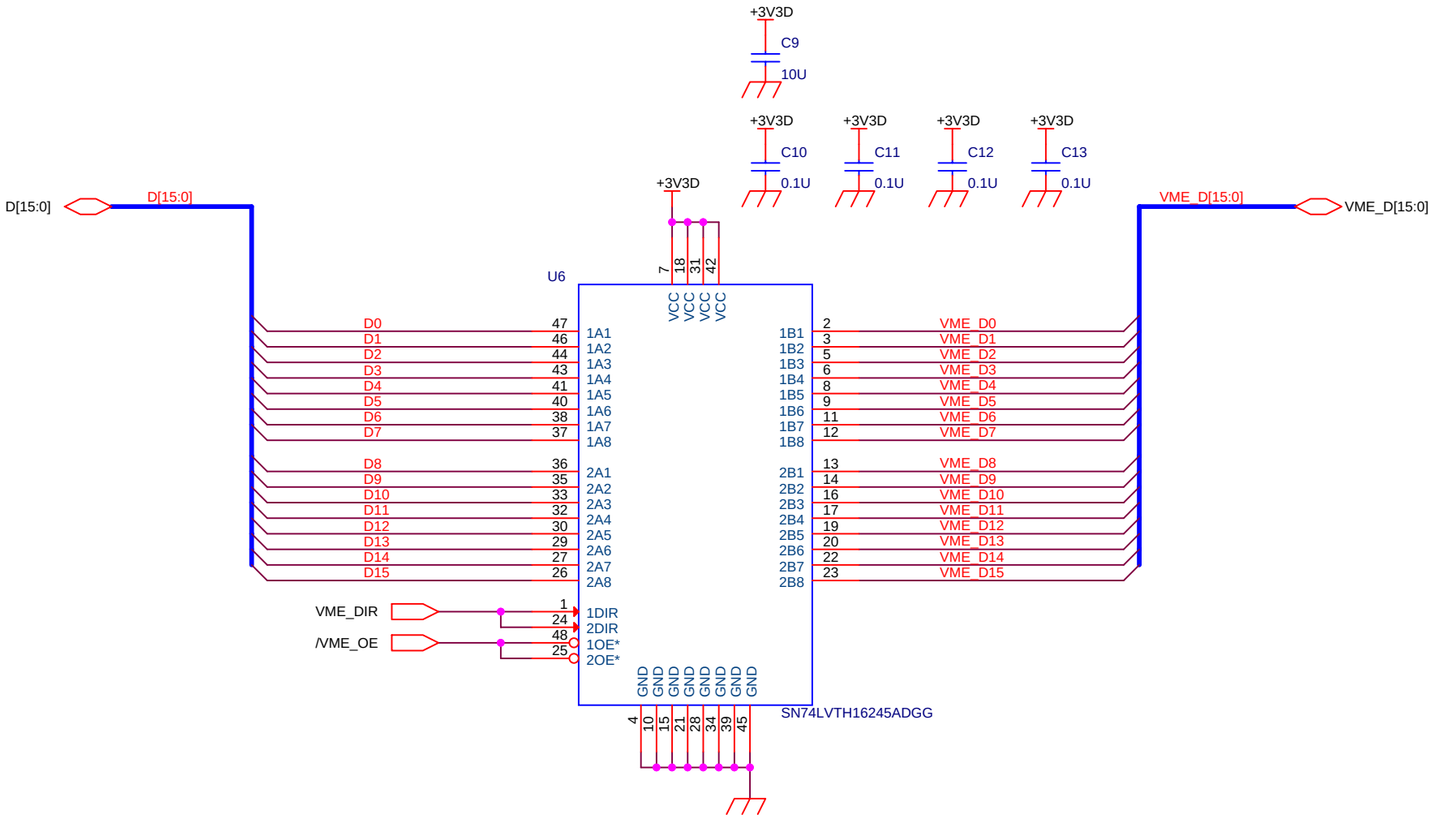
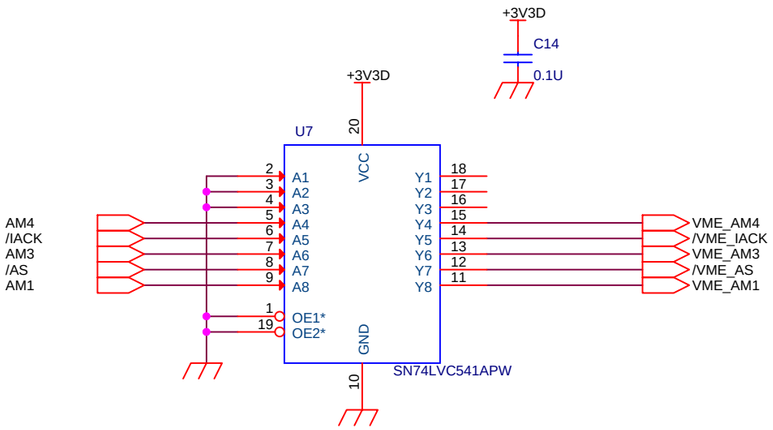
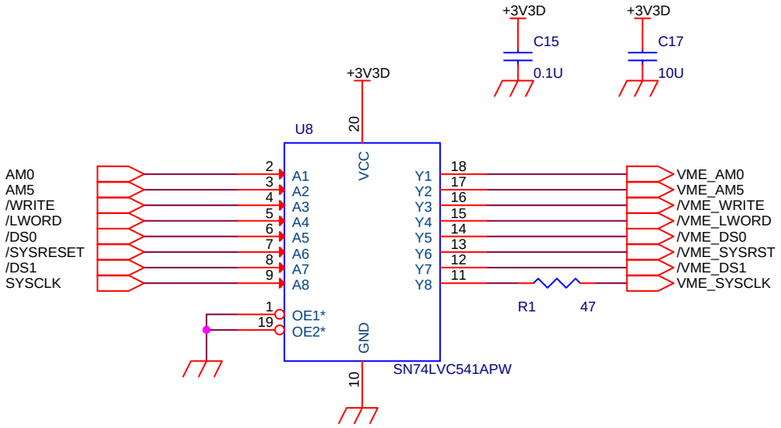
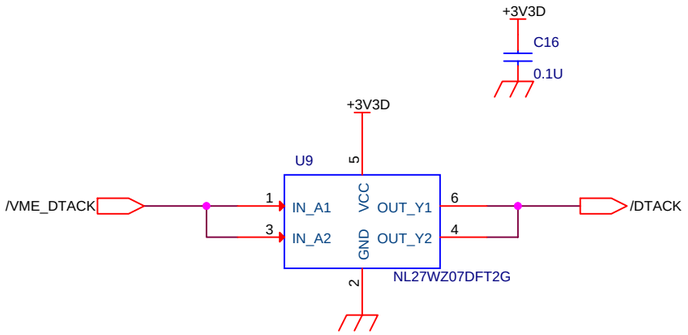
Date:	Monday, March 23, 2015
Sheet	3 of 18









OR_Module for burst stopper

Title: Data Buffer		
Size: A3	Document Number	Rev: 3.0
Date: Monday, March 23, 2015	Sheet 4 of 18	

CPLD TEST

CN4

XG4C-3431

+1V8D C18 10U

+1V8D C19 0.1U

+1V8D C20 0.1U

+1V8D C21 0.1U

+3V3D C22 0.1U · C23 0.1U · C24 0.1U · C25 0.1U · C26 0.1U · C27 0.1U · C28 0.1U · C29 0.1U · C30 0.1U · C31 0.1U · C32 0.1U · C33 0.1U · C35 0.1U

+3V3D C34 10U · C36 10U

RN3 4.7Kx4/3216

SW3 CHS-04B

U10

CoolRunner II CPLD

XC2C256-7PQ208C

CPLD JTAG

CN3 87831-1420

CPLD_TEST0	3	4	P0
CPLD_TEST1	5	6	P1
CPLD_TEST2	7	8	P2
CPLD_TEST3	9	10	P3
CPLD_TEST4	11	12	P4
CPLD_TEST5	13	14	P5
CPLD_TEST6	15	16	P6
CPLD_TEST7	17	18	P7
CPLD_TEST8	19	20	P8
CPLD_TEST9	21	22	P9
CPLD_TEST10	23	24	P10
CPLD_TEST11	25	26	P11
CPLD_TEST12	27	28	P12
CPLD_TEST13	29	30	P13
CPLD_TEST14	31	32	P14
CPLD_TEST15	33	34	P15

/CPLD_BPI_CE	/CPLD_BPI_CE	/CPLD_BPI_CE	/CPLD_BPI_CE
/CPLD_BPI_OE	/CPLD_BPI_OE	/CPLD_BPI_OE	/CPLD_BPI_OE
/CPLD_BPI_WE	/CPLD_BPI_WE	/CPLD_BPI_WE	/CPLD_BPI_WE
/CPLD_BPI_RST	/CPLD_BPI_RST	/CPLD_BPI_RST	/CPLD_BPI_RST
/CPLD_BPI_ADV	/CPLD_BPI_ADV	/CPLD_BPI_ADV	/CPLD_BPI_ADV
BPI_IN_SEL	BPI_IN_SEL	BPI_IN_SEL	BPI_IN_SEL
/BPI_IN_OE	BPI_IN_OE	BPI_IN_OE	/BPI_IN_OE
BPI_WAIT	BPI_WAIT	BPI_WAIT	BPI_WAIT
BPI_D_DIR	BPI_D_DIR	BPI_D_DIR	BPI_D_DIR
/BPI_D_OE	/BPI_D_OE	/BPI_D_OE	/BPI_D_OE
/BPI_A_OE	/BPI_A_OE	/BPI_A_OE	/BPI_A_OE
FPGA_M0	FPGA_M0	FPGA_M0	FPGA_M0
FPGA_M1	FPGA_M1	FPGA_M1	FPGA_M1
FPGA_M2	FPGA_M2	FPGA_M2	FPGA_M2
/FPGA_INIT	/FPGA_INIT	/FPGA_INIT	/FPGA_INIT
FPGA_CCLK	FPGA_CCLK	FPGA_CCLK	FPGA_CCLK
FPGA_TMS	FPGA_TMS	FPGA_TMS	FPGA_TMS
FPGA_TCK	FPGA_TCK	FPGA_TCK	FPGA_TCK
FPGA_TDO	FPGA_TDO	FPGA_TDO	FPGA_TDO
FPGA_TDI	FPGA_TDI	FPGA_TDI	FPGA_TDI
/FPGA_PROG	/FPGA_PROG	/FPGA_PROG	/FPGA_PROG
FPGA_DONE	FPGA_DONE	FPGA_DONE	FPGA_DONE
/FPGA_RDWR	/FPGA_RDWR	/FPGA_RDWR	/FPGA_RDWR
/FPGA_CSI	/FPGA_CSI	/FPGA_CSI	/FPGA_CSI
/FPGA_RESET	/FPGA_RESET	/FPGA_RESET	/FPGA_RESET
/FPGA_STATE	/FPGA_STATE	/FPGA_STATE	/FPGA_STATE
/FPGA_WSTR	/FPGA_WSTR	/FPGA_WSTR	/FPGA_WSTR
/FPGA_RSTR	/FPGA_RSTR	/FPGA_RSTR	/FPGA_RSTR
/FPGA_OE0	/FPGA_OE0	/FPGA_OE0	/FPGA_OE0
/FPGA_OE1	/FPGA_OE1	/FPGA_OE1	/FPGA_OE1
FPGA_CCLK_OUT	FPGA_CCLK_OUT	FPGA_CCLK_OUT	FPGA_CCLK_OUT
P_GOOD0	P_GOOD0	P_GOOD0	P_GOOD0
P_GOOD1	P_GOOD1	P_GOOD1	P_GOOD1
SPARE0	SPARE0	SPARE0	SPARE0
SPARE1	SPARE1	SPARE1	SPARE1
SPARE2	SPARE2	SPARE2	SPARE2
SPARE3	SPARE3	SPARE3	SPARE3
SPARE4	SPARE4	SPARE4	SPARE4
SPARE5	SPARE5	SPARE5	SPARE5
SPARE6	SPARE6	SPARE6	SPARE6
SPARE7	SPARE7	SPARE7	SPARE7

CPLD_CLK	CPLD_CLK	IO_GCK0	45
		IO_GCK1	47
		IO_GCK2	55
		IO_CDR	51
		IO_DGE	60
CPLD_TDI	CPLD_TDI	TDI	95
CPLD_TMS	CPLD_TMS	TMS	96
CPLD_TCK	CPLD_TCK	TCK	98

CPLD_TEST0	9	IO_GTS1	8
CPLD_TEST1	10	IO_GTS2	3
CPLD_TEST2	12	IO_GTS3	6
CPLD_TEST3	14	IO_GTS0	7
CPLD_TEST4	15		
CPLD_TEST5	16		
CPLD_TEST6	17		
CPLD_TEST7	18		
CPLD_TEST8	19		
CPLD_TEST9	20		
CPLD_TEST10	21		
CPLD_TEST11	22		
CPLD_TEST12	23		
CPLD_TEST13	25		
CPLD_TEST14	27		
CPLD_TEST15	28		
FPGA_TDO	32		
FPGA_TDI	33		
FPGA_TMS	34		
FPGA_TCK	35		
FPGA_M0	36		
FPGA_M1	37		
FPGA_M2	38		
FPGA_DONE	39		
FPGA_CCLK	40		
/FPGA_RSTR	56		
/FPGA_OE1	57		
/CPLD_BPI_ADV	58		
/FPGA_RESET	60		
/FPGA_OE0	61		
/FPGA_STATE	62		
BPI_IN_OE	63		
/CPLD_BPI_WE	64		
/CPLD_BPI_RST	65		
/FPGA_INIT	66		
/FPGA_WSTR	69		
BPI_IN_SEL	70		
/CPLD_BPI_CE	71		
P_GOOD0	80		
P_GOOD1	82		
/CPLD_BPI_OE	85		
FPGA_CCLK_OUT	86		
BPI_WAIT	87		
BPI_D_DIR	88		
/FPGA_RDWR	89		
/FPGA_CSI	90		
/FPGA_PROG	91		

CPLD_M0	205	/P_RESET	
CPLD_M1	203		
CPLD_M2	202		
CPLD_M3	201		
VME_D0	200		
VME_D1	199		
VME_D2	198		
VME_D3	197		
VME_D4	196		
VME_D5	195		
VME_D6	194		
VME_D7	193		
VME_D8	192		
VME_D9	191		
VME_D10	189		
VME_D11	188		
VME_D12	187		
VME_D13	186		
VME_D14	185		
VME_D15	184		
VME_DIR	183		
/VME_OE	182		
VME_SYSCLK	180		
/VME_DS1	179		
/VME_SYSRST	178		
CPLD_TDO	176		
/VME_DS0	175		
/VME_LWORD	174		
/VME_WRITE	173		
VME_AM5	171		
VME_AM0	170		
/VME_DTACK	169		
VME_AM1	168		
/VME_AS	167		
VME_AM3	166		
/VME_IACK	165		
VME_AM4	164		
VME_A23	163		
VME_A22	162		
VME_A21	161		
VME_A20	160		
VME_A19	159		
VME_A18	158		
VME_A17	155		
VME_A16	154		
VME_A15	153		
VME_A14	152		
VME_A13	151		
VME_A12	150		
VME_A11	149		
VME_A10	148		
VME_A9	147		
VME_A8	146		
VME_A7	145		
VME_A6	144		
VME_A5	143		
VME_A4	142		
VME_A3	140		
VME_A2	139		
VME_A1	138		
FIXED_SPARE2	137		
FIXED_SPARE1	136		
FIXED_SPARE0	135		
/VME_MATCH	134		
VME_A25	128		
VME_A24	127		
SPARE7	126		
SPARE6	125		
SPARE5	123		
VME_A26	122		
/BPI_A_OE	121		
SPARE1	120		
SPARE0	119		
SPARE4	118		
SPARE3	117		
SPARE2	116		
/BPI_D_OE	106		

VME_A26	VME_A25	VME_A24	VME_A23
VME_A22	VME_A21	VME_A20	VME_A19
VME_A18	VME_A17	VME_A16	VME_A15
VME_A14	VME_A13	VME_A12	VME_A11
VME_A10	VME_A9	VME_A8	VME_A7
VME_A6	VME_A5	VME_A4	VME_A3
VME_A2	VME_A1		

VME_A[26:1] → VME_A[26:1]

VME_D15	VME_D14	VME_D13	VME_D12
VME_D11	VME_D10	VME_D9	VME_D8
VME_D7	VME_D6	VME_D5	VME_D4
VME_D3	VME_D2	VME_D1	VME_D0

VME_D[15:0] → VME_D[15:0]

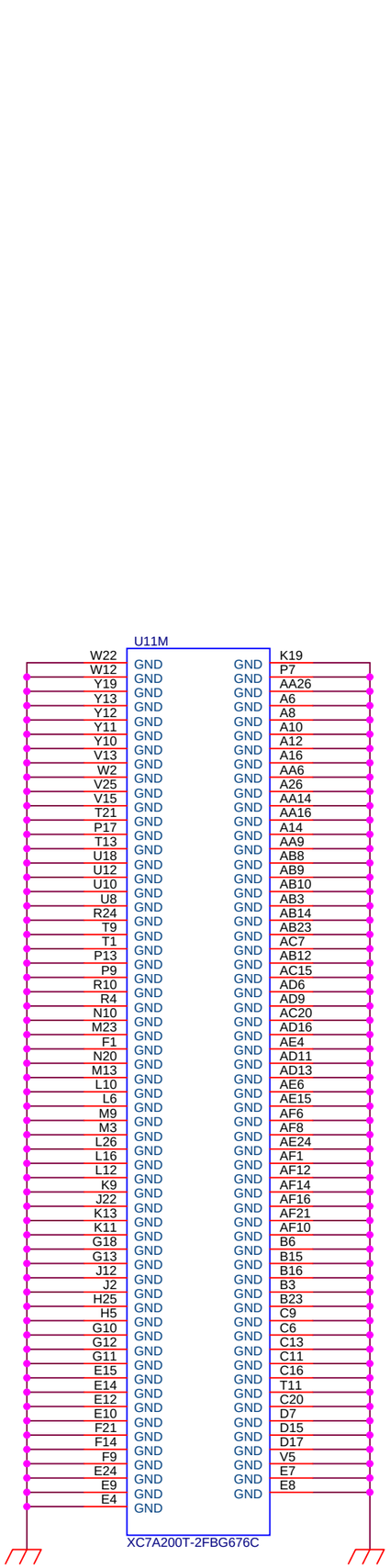
FIXED_SPARE0	FIXED_SPARE0	FIXED_SPARE0
FIXED_SPARE1	FIXED_SPARE1	FIXED_SPARE1
FIXED_SPARE2	FIXED_SPARE2	FIXED_SPARE2

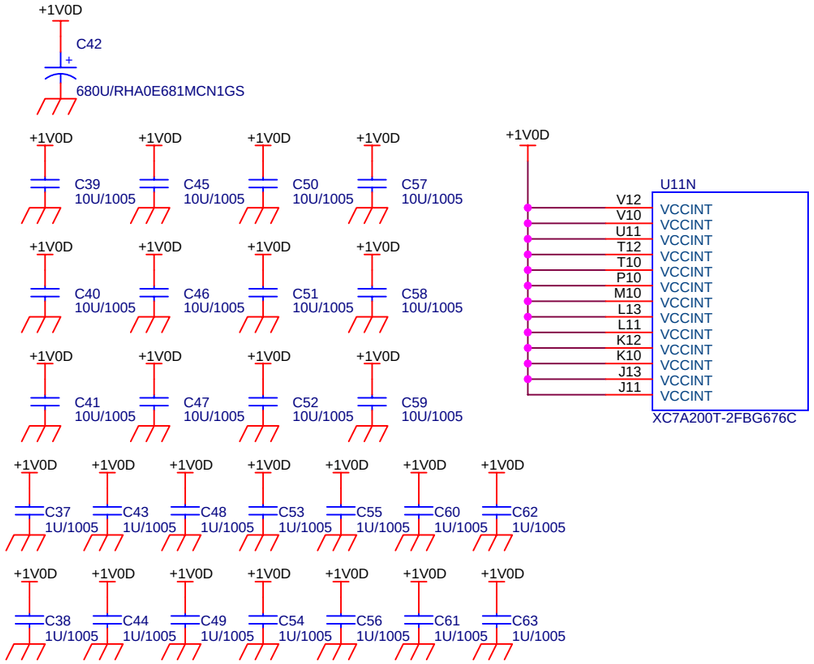
VME_DIR	VME_DIR	VME_DIR	VME_DIR
/VME_OE	/VME_OE	/VME_OE	/VME_OE
VME_SYSCLK	VME_SYSCLK	VME_SYSCLK	VME_SYSCLK
/VME_DS1	/VME_DS1	/VME_DS1	/VME_DS1
/VME_SYSRST	/VME_SYSRST	/VME_SYSRST	/VME_SYSRST
/VME_DS0	/VME_DS0	/VME_DS0	/VME_DS0
/VME_LWORD	/VME_LWORD	/VME_LWORD	/VME_LWORD
/VME_WRITE	/VME_WRITE	/VME_WRITE	/VME_WRITE
VME_AM5	VME_AM5	VME_AM5	VME_AM5
VME_AM0	VME_AM0	VME_AM0	VME_AM0
/VME_DTACK	/VME_DTACK	/VME_DTACK	/VME_DTACK
VME_AM1	VME_AM1	VME_AM1	VME_AM1
/VME_AS	/VME_AS	/VME_AS	/VME_AS
VME_AM3	VME_AM3	VME_AM3	VME_AM3
/VME_IACK	/VME_IACK	/VME_IACK	/VME_IACK
VME_AM4	VME_AM4	/VME_MATCH	/VME_MATCH

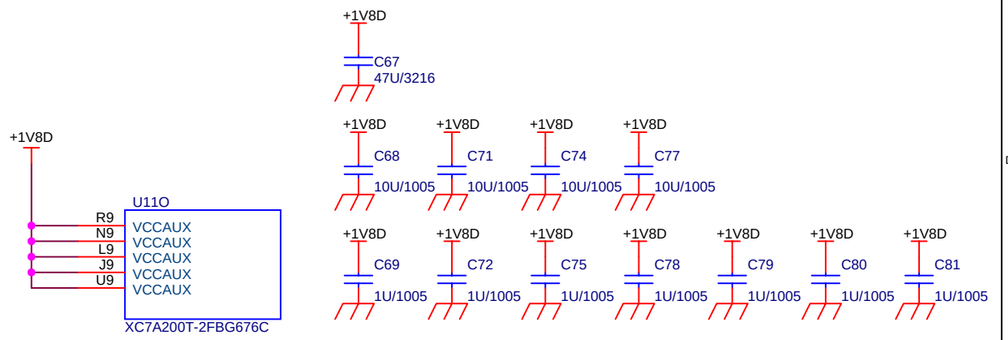
+1V8D	1	53	124												
+3V3D	11	33	59	79	92	105	132	133	157	172	181	204	26		
	VAUX	VCCIO1	VCCIO1	VCCIO1	VCCIO1	VCCIO1	VCCIO1	VCCIO2	VCCIO2	VCCIO2	VCCIO2	VCCIO2	VCCIO2		
	VCC	VCC	VCC												
GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND		
13	24	42	52	68	81	93	104	129	130	141	156	177	190	207	

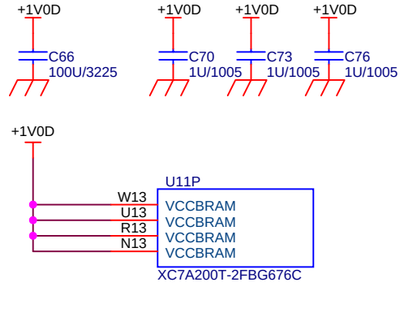
VCC	1	GND	VCC	2	+3V3D
TMS	3	GND	TMS	4	CPLD_TMS
TCK	5	GND	TCK	6	CPLD_TCK
TDO	7	GND	TDO	8	CPLD_TDO
TDI	9	GND	TDI	10	CPLD_TDI
	11	GND	NC	12	
	13	GND	NC	14	

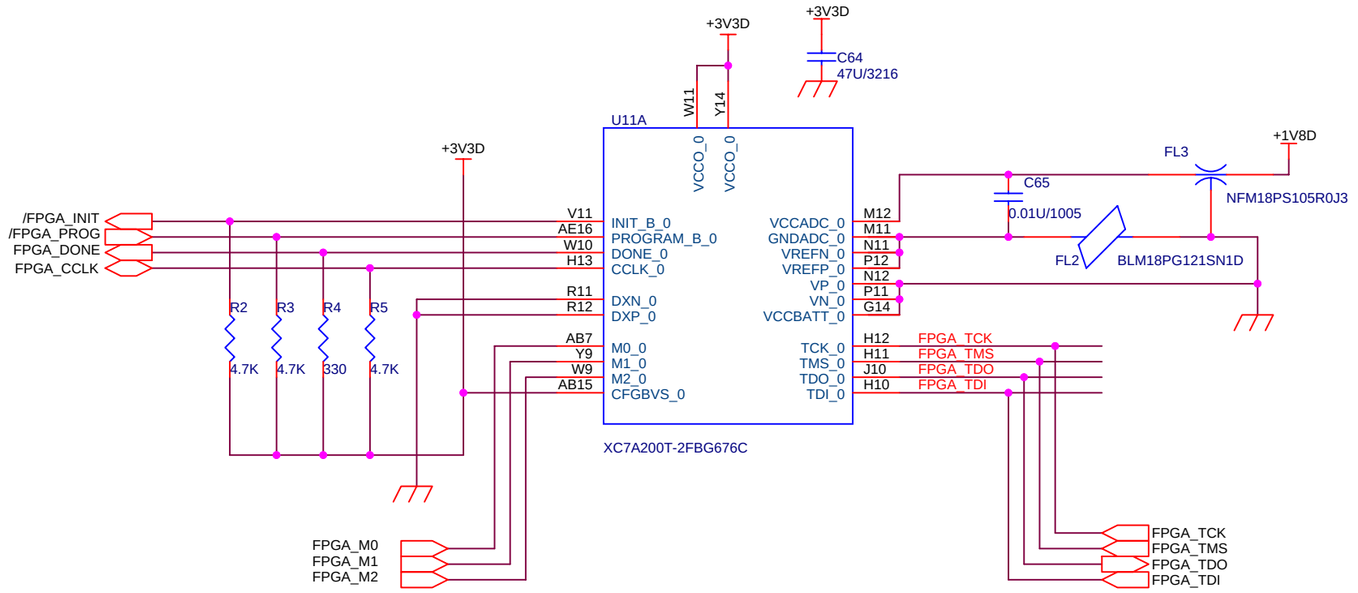
Title	CoolRunner II CPLD		
Size A3	Document Number	OR_Module for burst stopper	Rev 3.0
Date:	Monday, March 23, 2015	Sheet 5 of 18	



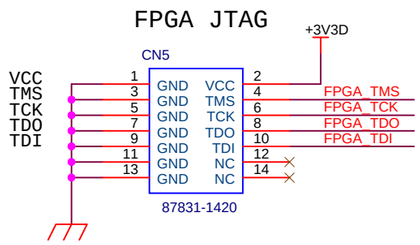






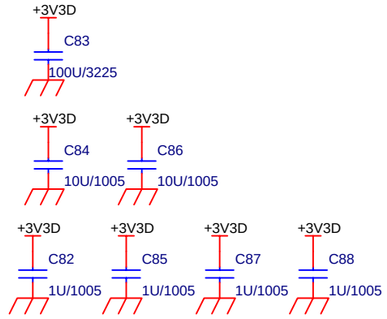


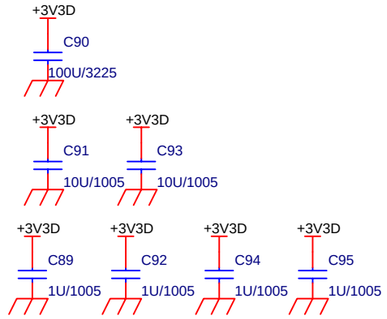
M0,M1,M2 でコンフィギュレーションモードを決める



OR_Module for burst stopper

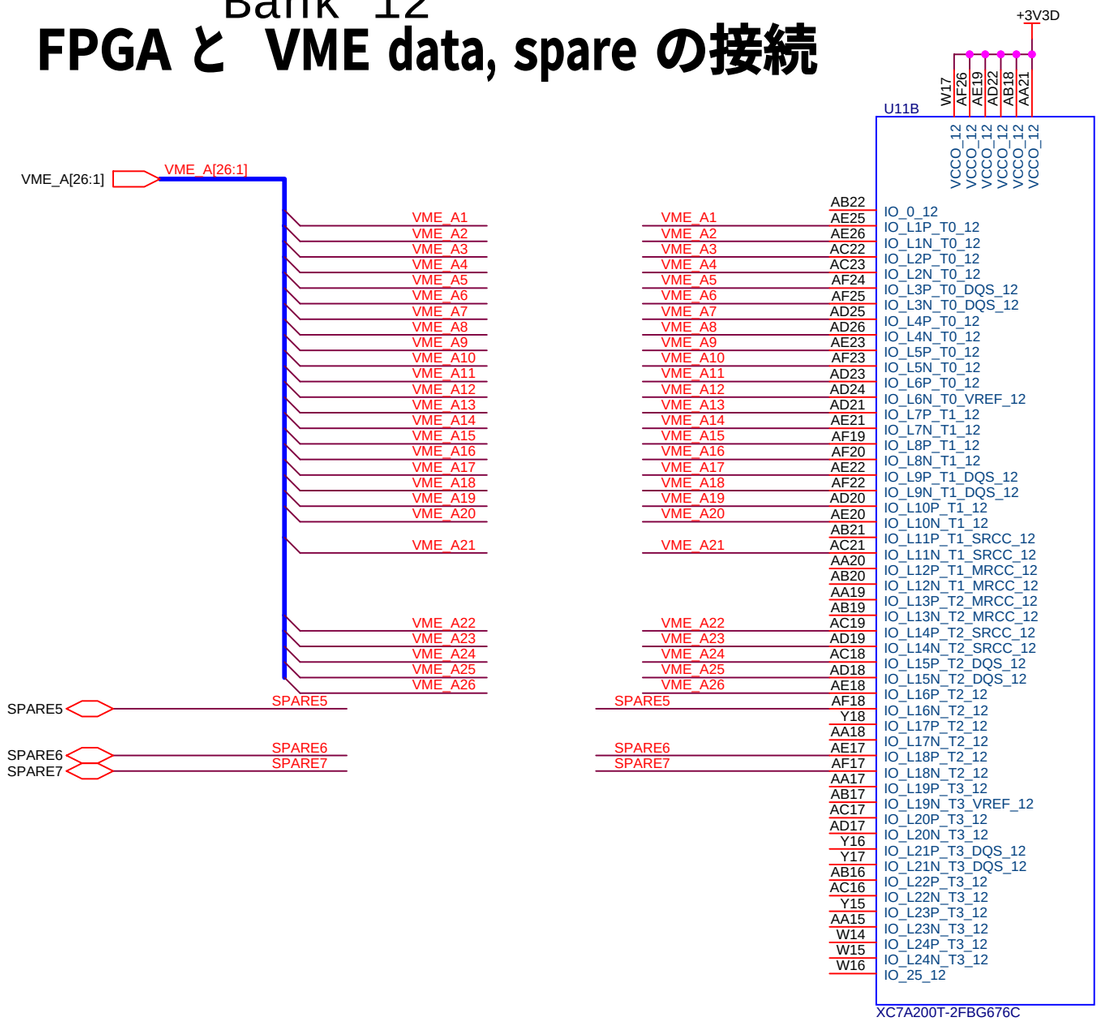
Title	FPGA Bank0,GND for PWR	
Size A3	Document Number	Rev 3.0
Date: Monday, March 23, 2015	Sheet 6 of 18	





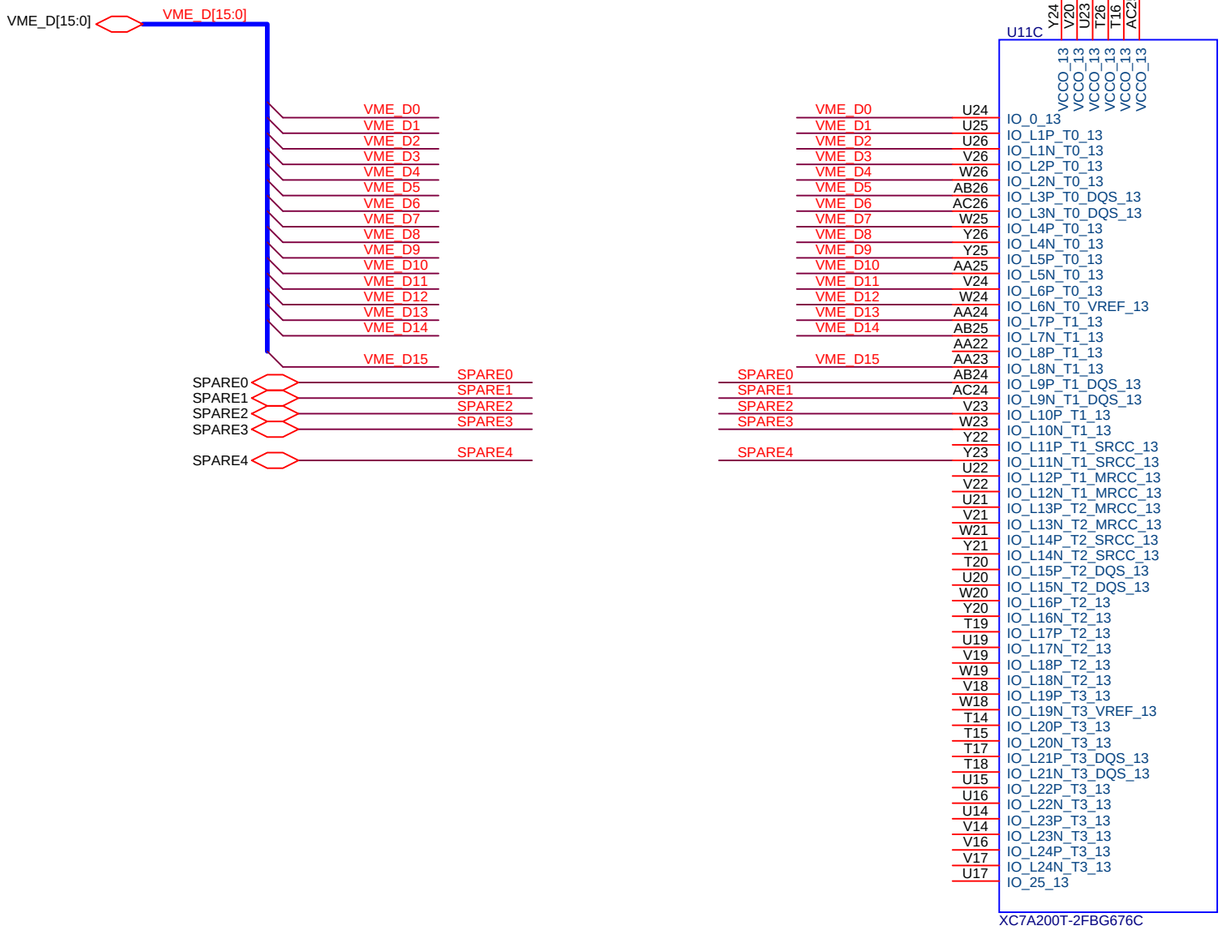
Bank 12

FPGA と VME data, spare の接続



Bank 13

FPGA と VME address, spare の接続



OR_Module for burst stopper		
Title: FPGA Bank 12,13 for VME, SPARE		
Size: A3	Document Number	Rev: 3.0
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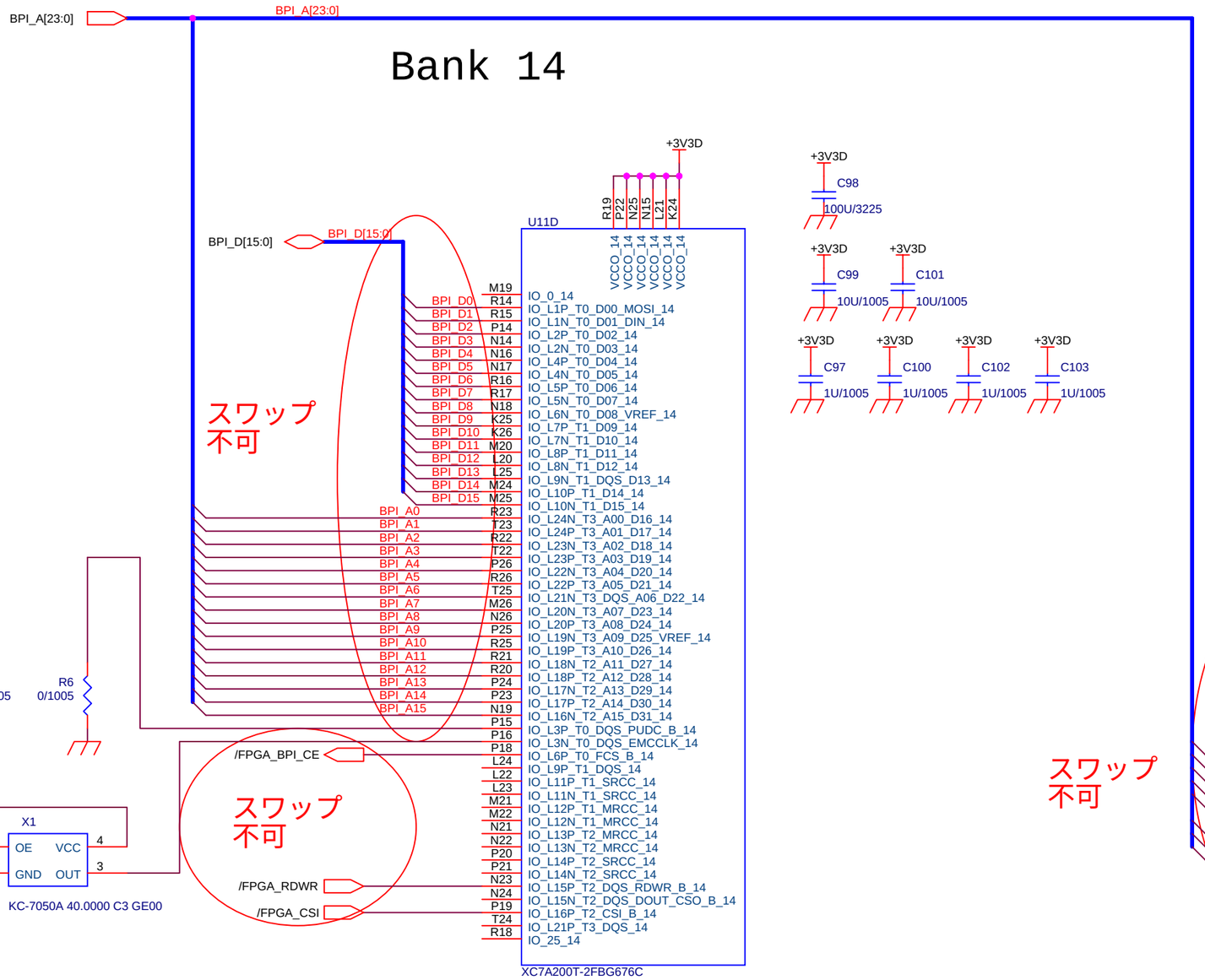
for PROM



OR_Module for burst stopper		
Title: FPGA Bank14,15 for PROM		
Size: A3	Document Number: <Doc>	Rev: 3.0
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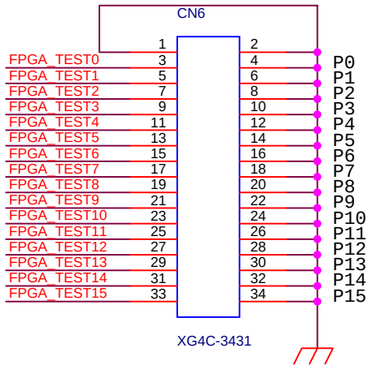
for TESTPIN

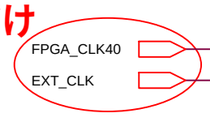
Bank 16

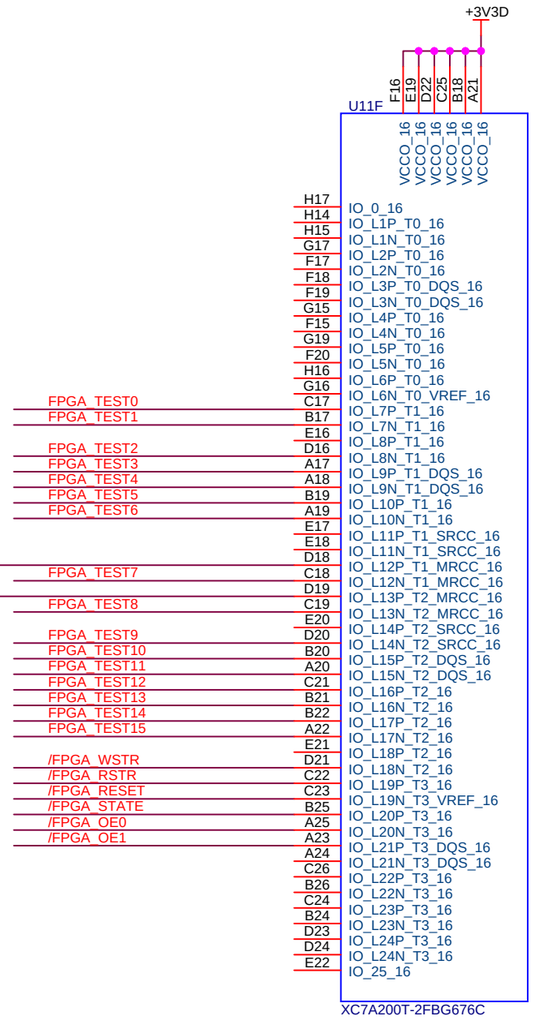
FPGA と TESTPIN, CPLD の接続

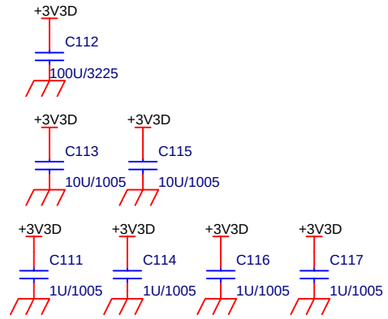
FPGA_TEST



本ページ中これらの信号だけ
スワップ不可
これら以外はスワップ可能







Title	FPGA Bank16 for TESTPIN,CPLD	
Size A3	Document Number <Doc>	Rev 3.0
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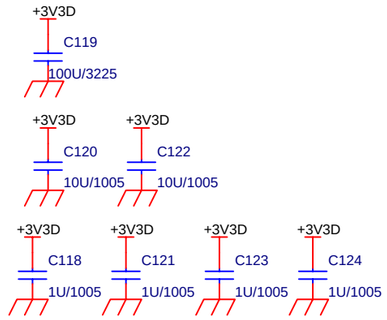
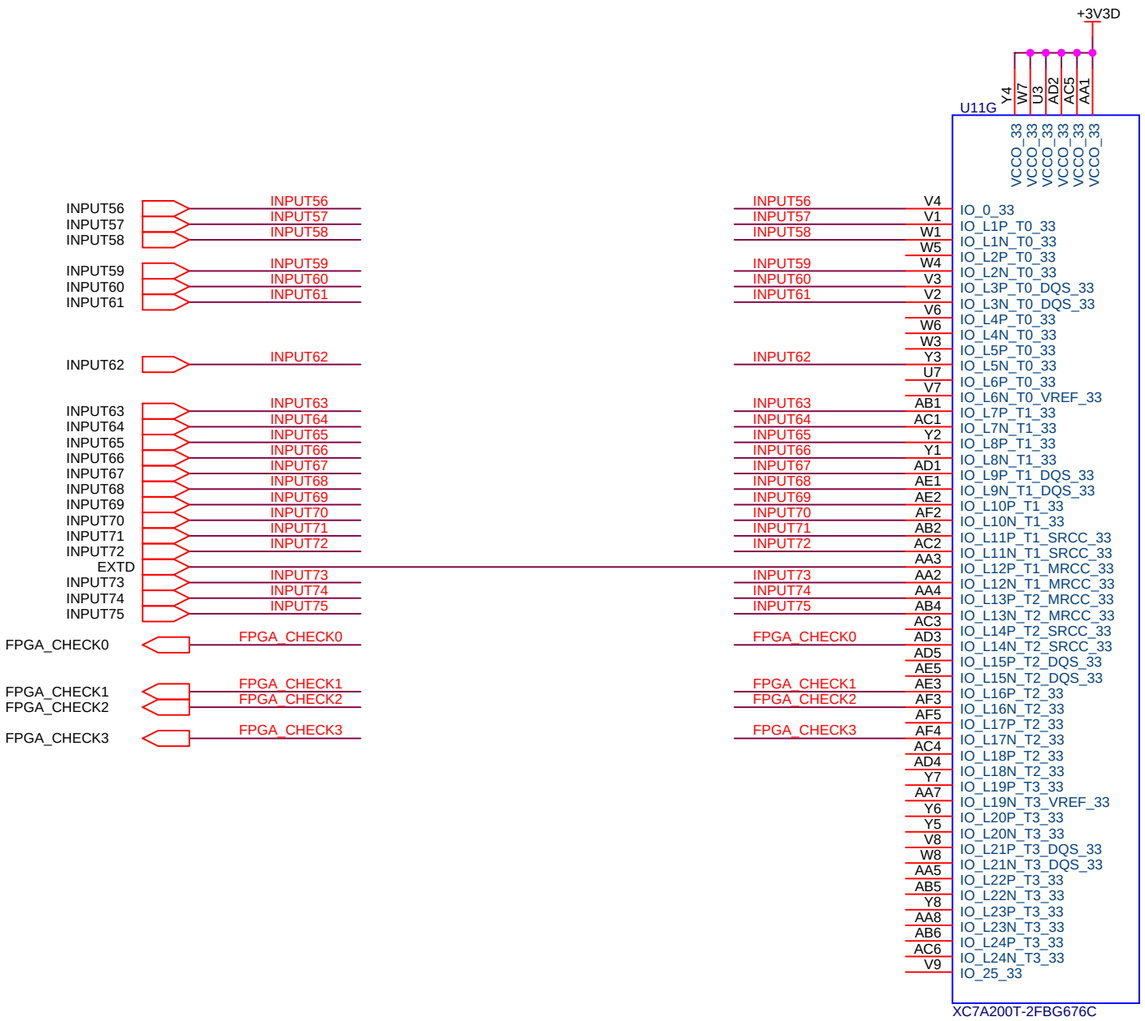
OR_Module for burst stopper

Bank 33

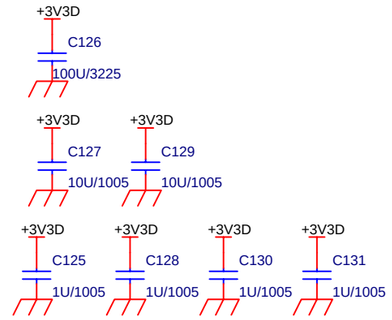
FPGA と INPUT の接続

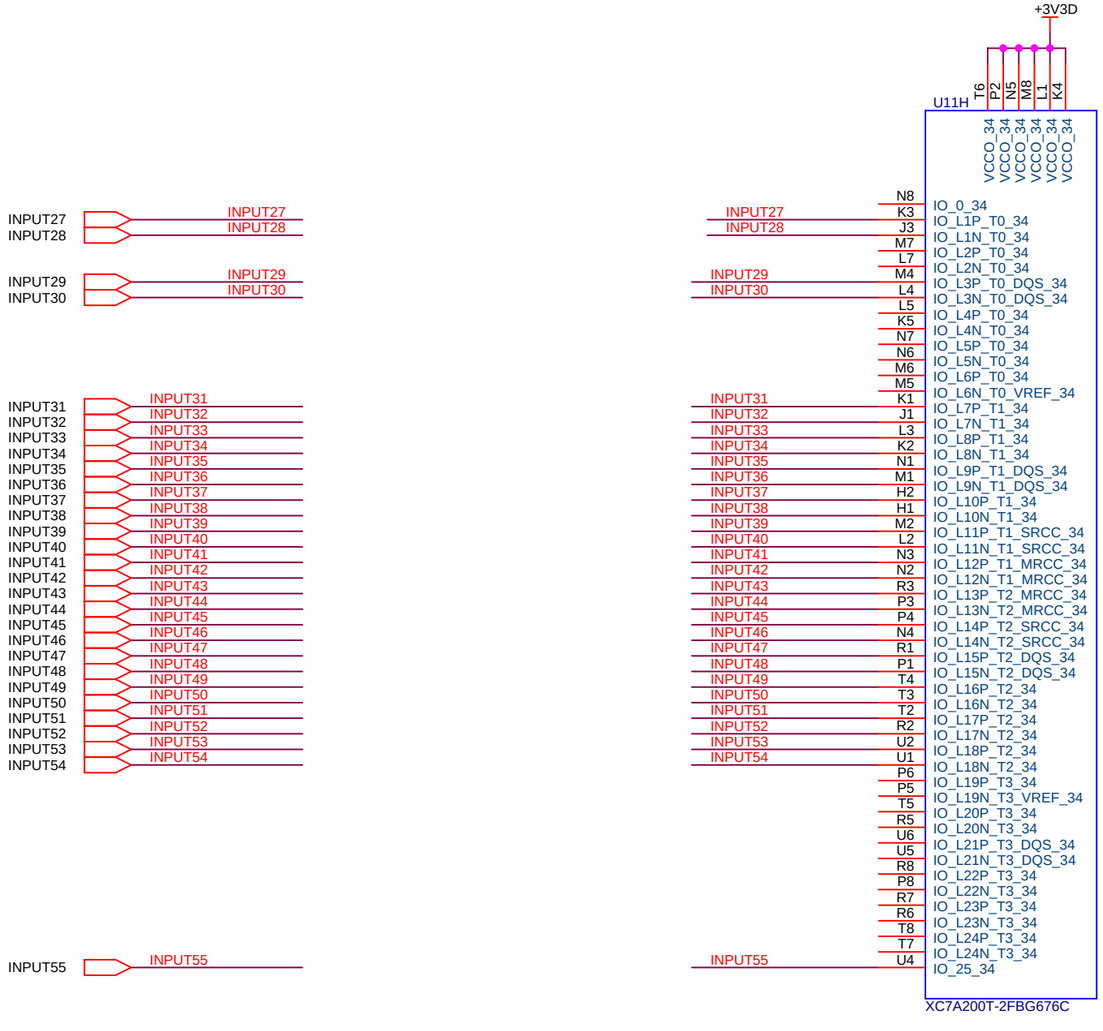




Bank 34

FPGA と INPUT の接続





OR_Module for burst stopper		
Title: FPGA Bank33,34 for INPUT		
Size: A3	Document Number: <Doc>	Rev: 3.0
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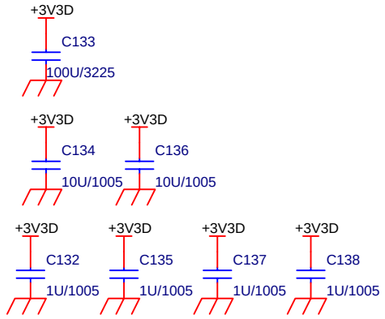
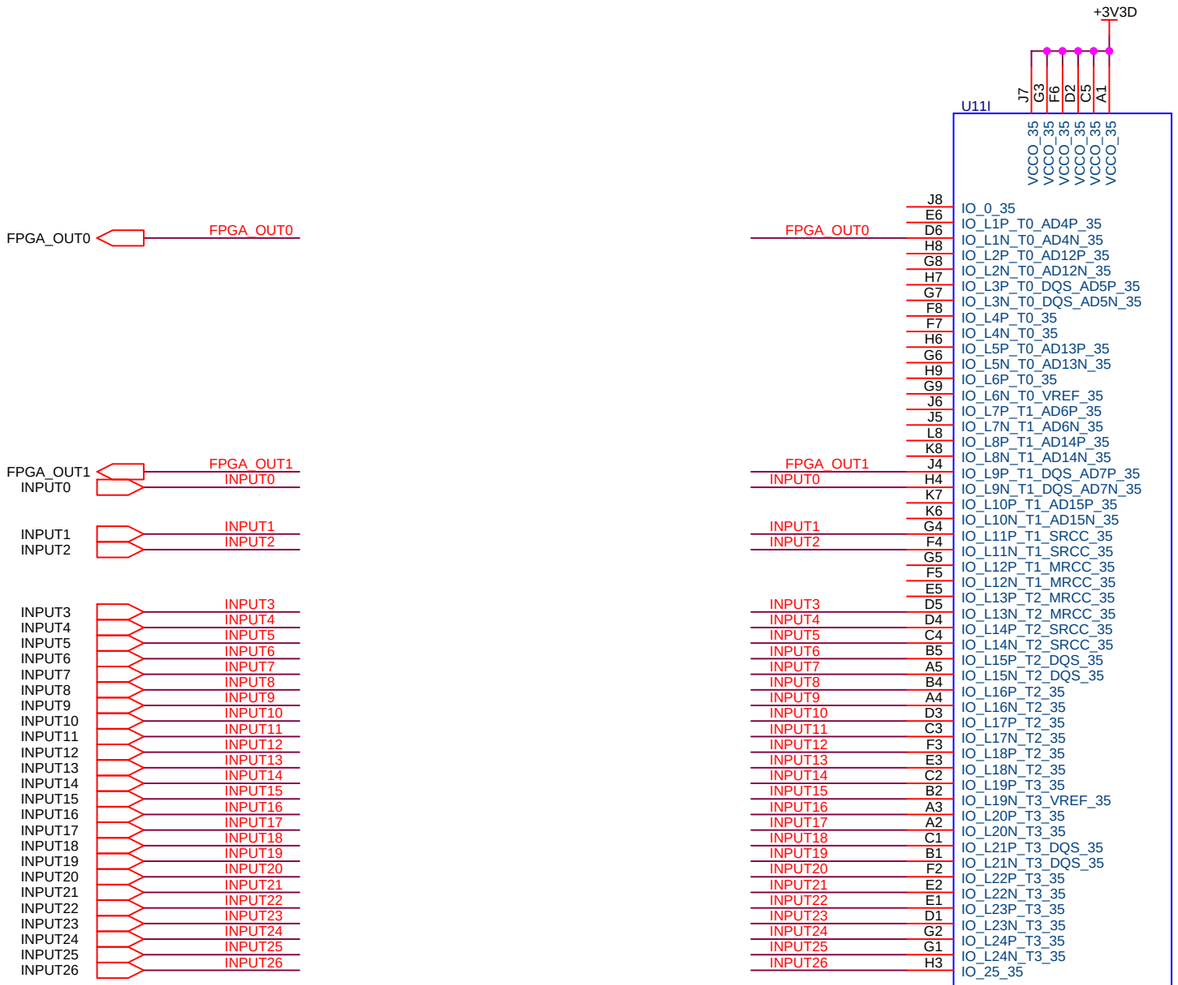
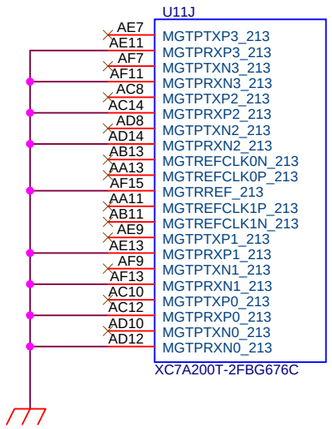
Bank 35

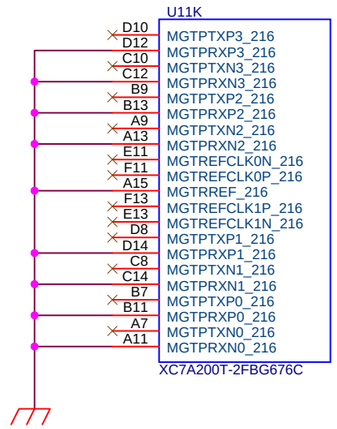
FPGA と INPUT,OUTPUT の接続

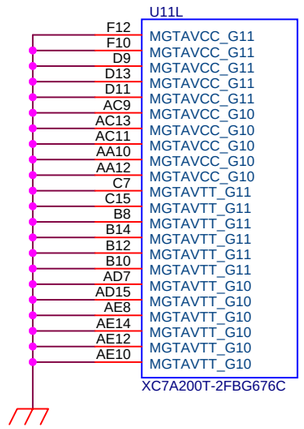




OR_Module for burst stopper		
Title: FPGA Bank35 for INPUT, OUTPUT		
Size: A3	Document Number: <Doc>	Rev: 3.0
Date: Monday, March 23, 2015	Sheet 11 of 18	







for GTP

OR_Module for burst stopper		
Title: FPGA Bank 213,216 for GTP		
Size: A3	Document Number: <Doc>	Rev: 3.0
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CMOS 40.08MHz

+3V3D
FL4
NFM18PS105R0J3
C145
0.1U
X2
1 OE
2 GND
VDD 4
OUT 3
MXO3-7050C-40.079MHz
R15 47 FPGA_CLK40
R16 47

Clock Input

-3V3D
R7
3K
R8
390
C140
0.1U
+3V3D
C146
0.1U
+3V3D
C148
10U
U13
VCC 1
1A 8
1B 7
2A 6
2B 5
GND 4
1Y 2
2Y 3
SN65LVDS34D
R17 47
R18 47 EXT_CLK
R19 47 EXTD

CLK 1-2:INT CLK
3-4:EXT CLK
1
2 CPLD_CLK
3
JSW 1X3
J1

CN7
6 3 LOW
5 4 UP
1
2
LEMO_DUAL
EXTCLK
EXTD
R9 51
R10 51

-3V3D
C143
10U
+3V3D
C147
10U
-3V3D
C141
0.1U
+3V3D
C139
0.1U
U14
1 VEE
2 D
3 NC
4 NC
VCC 8
Q 7
Q* 6
GND 5
MC100EPT24DG
FPGA_OUT0
-3V3D
R12 150
-3V3D
R14 150
U16
1 NC
2 A
3 B
4 VBB
VCC 8
Y 7
Z 6
GND 5
SN65CML100D
-3V3D
C152
10U
-3V3D
C150
0.1U
-3V3D
R21 51
CN8
1 6 3 LOW
2 5 4 UP
OUT1
OUT2
LEMO_DUAL
-3V3D
C151
0.1U
-3V3D
C149
0.1U
-3V3D
C144
0.1U
+3V3D
C142
0.1U
U12
MC100EPT24DG
FPGA_OUT1
-3V3D
R11 150
-3V3D
R13 150
U15
SN65CML100D
-3V3D
R20 51

OR_Module for burst stopper			
Title: NIMCLOCK,NIMOUT			
Size: A3	Document Number		Rev: 3.0
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-3V3D
R94
3K
R95
390
C173
0.1U
C175
0.1U
C177
10U
C179
0.1U
C181
0.1U
+3V3D
CN27 LEMO_DUAL
CN28 LEMO_DUAL
CN31 LEMO_DUAL
CN32 LEMO_DUAL
U25
U27
SN65LVDS348PW
RIN1-
RIN1+
RIN2+
RIN2-
RIN3-
RIN3+
RIN4+
RIN4-
VCC
GND
EN
EN*
ROUT1
ROUT2
ROUT3
ROUT4
INPUT0
INPUT1
INPUT2
INPUT3
INPUT8
INPUT9
INPUT10
INPUT11
R100 47 INPUT_DUMP0
R101 47 INPUT_DUMP1
R102 47 INPUT_DUMP2
R103 47 INPUT_DUMP3
R120 47 INPUT_DUMP8
R121 47 INPUT_DUMP9
R122 47 INPUT_DUMP10
R123 47 INPUT_DUMP11
INPUT_DUMP0
INPUT_DUMP1
INPUT_DUMP2
INPUT_DUMP3
INPUT_DUMP8
INPUT_DUMP9
INPUT_DUMP10
INPUT_DUMP11
R90 R92 R96 R99
R108 R110 R112 R114
51
LOW
UP
CN35
XG8W-3431
P0
P1
P2
P3
P4
P5
P6
P7
P8
P9
P10
P11
P12
P13
P14
P15
C174
0.1U
C176
0.1U
C178
10U
C180
0.1U
C182
0.1U
CN29 LEMO_DUAL
CN30 LEMO_DUAL
CN33 LEMO_DUAL
CN34 LEMO_DUAL
U26
U28
INPUT4
INPUT5
INPUT6
INPUT7
INPUT12
INPUT13
INPUT14
INPUT15
R104 47 INPUT_DUMP4
R105 47 INPUT_DUMP5
R106 47 INPUT_DUMP6
R107 47 INPUT_DUMP7
R116 47 INPUT_DUMP12
R117 47 INPUT_DUMP13
R118 47 INPUT_DUMP14
R119 47 INPUT_DUMP15
INPUT_DUMP4
INPUT_DUMP5
INPUT_DUMP6
INPUT_DUMP7
INPUT_DUMP12
INPUT_DUMP13
INPUT_DUMP14
INPUT_DUMP15
R91 R93 R97 R98
R109 R111 R113 R115

OR_Module for burst stopper

Title	NIM	
Size A3	Document Number <Doc>	Rev 3.0
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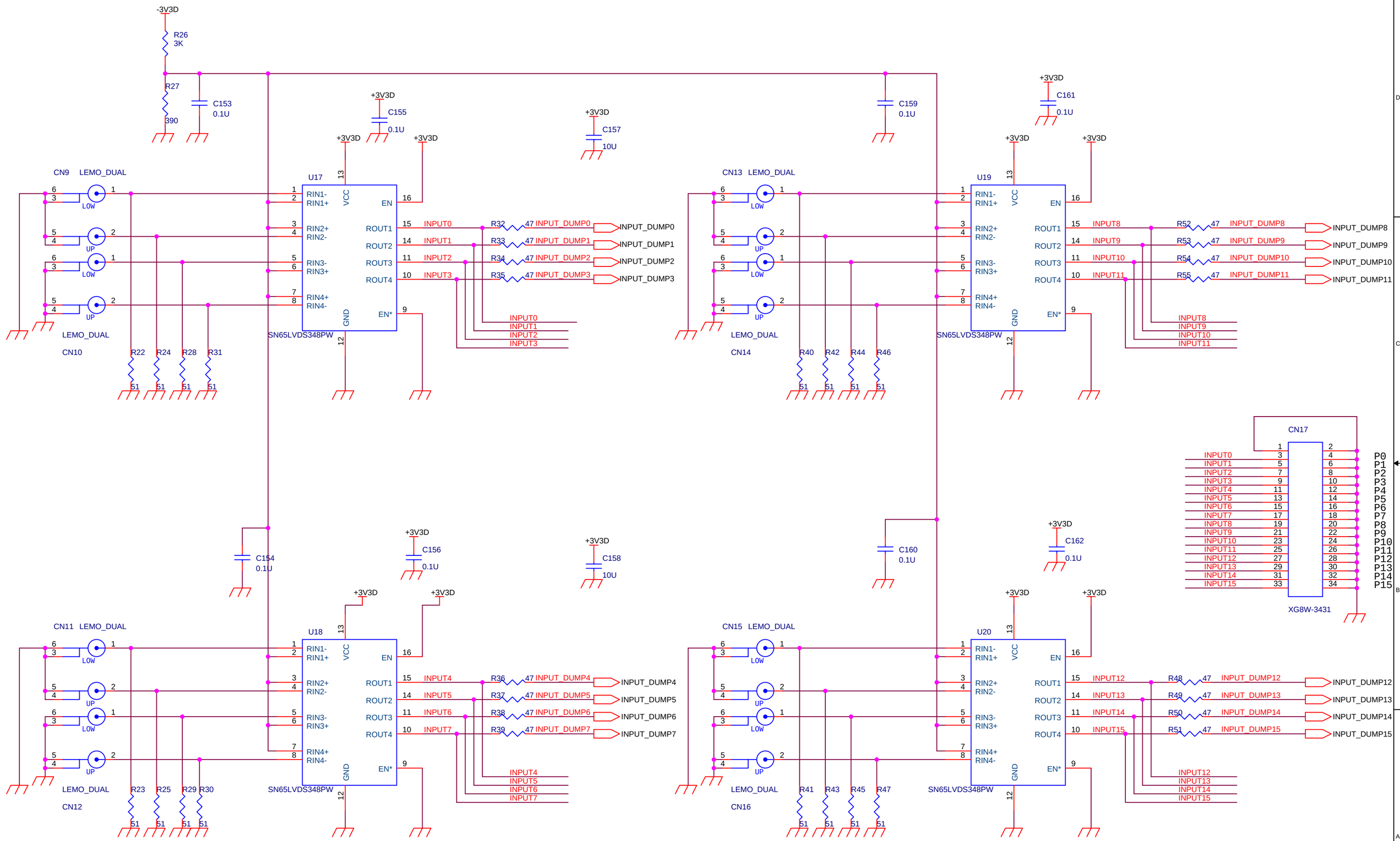
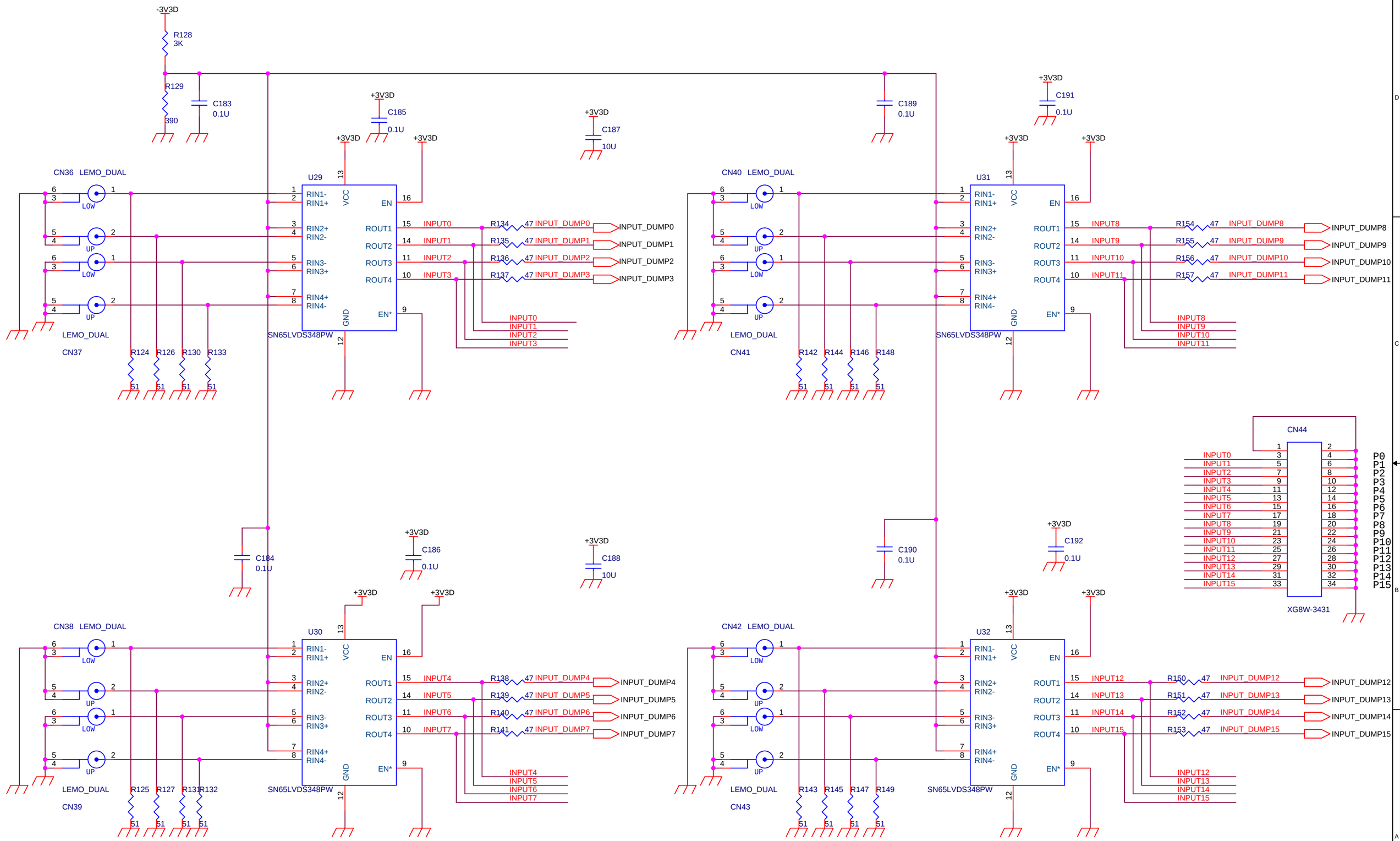


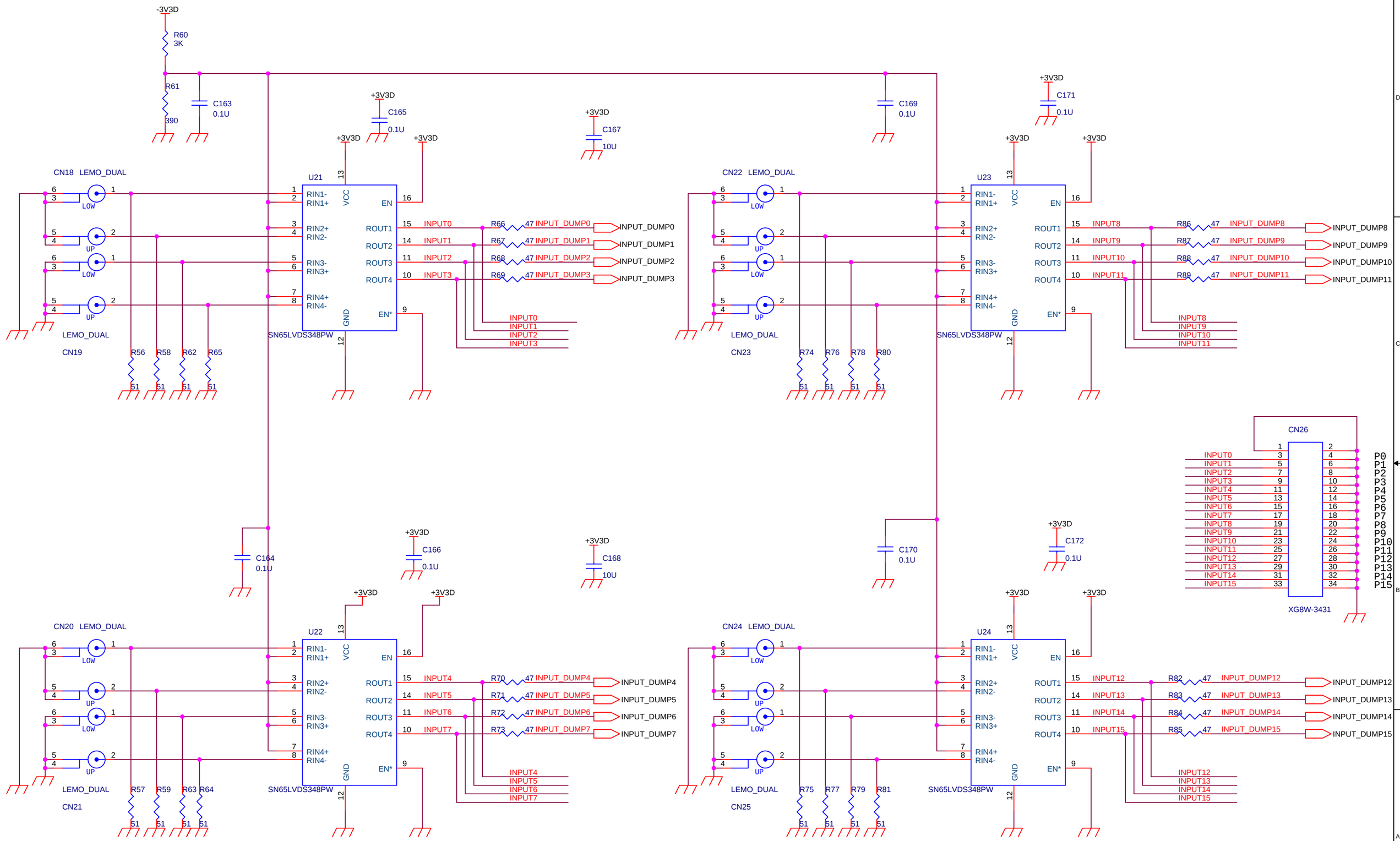
Title	NIM	
Size A3	Document Number <Doc>	Rev 3.0
Date: Monday, March 23, 2015	Sheet 14 of 18	

OR_Module for burst stopper



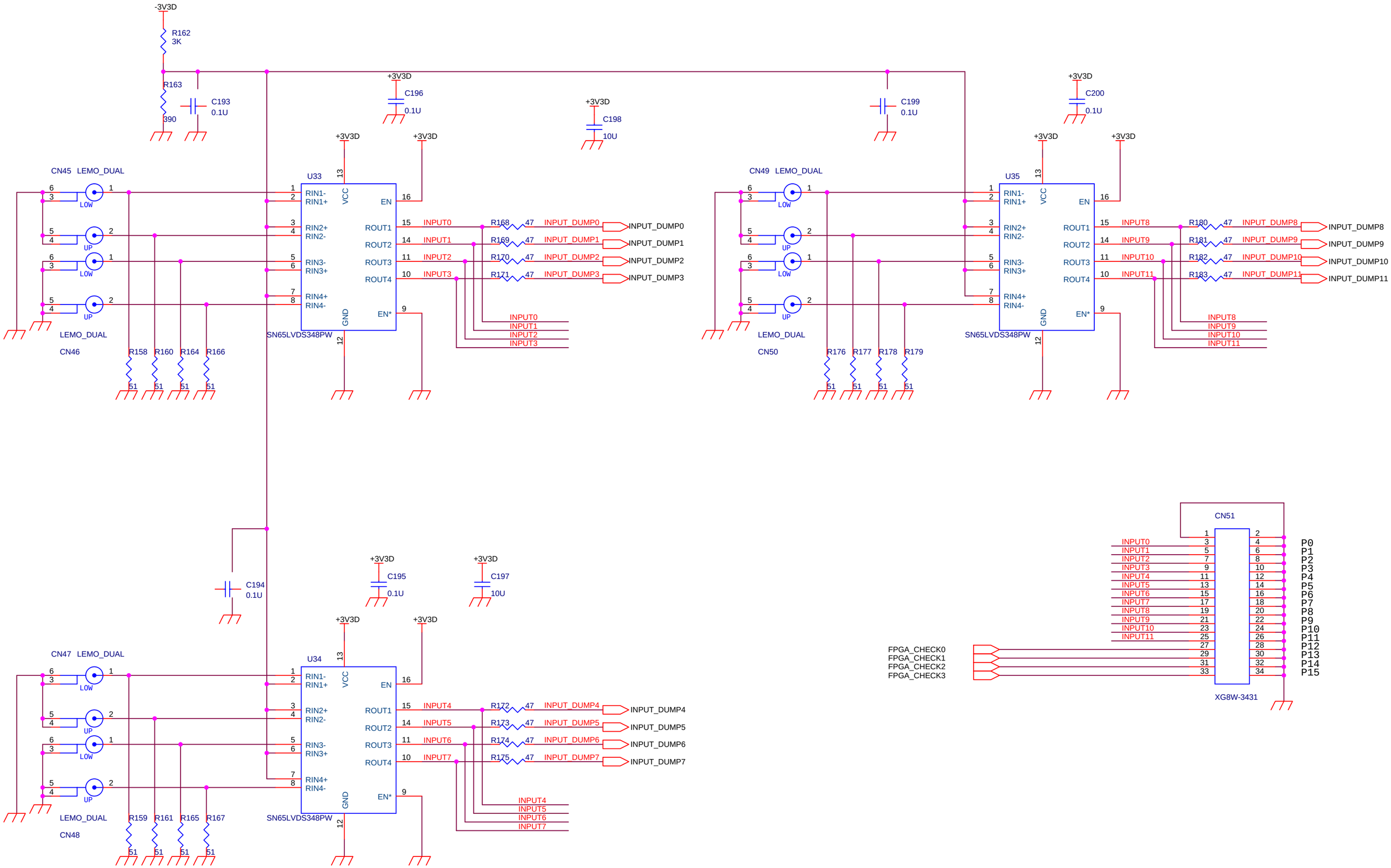
Title	NIM	
Size A3	Document Number <Doc>	Rev 3.0
Date: Monday, March 23, 2015	Sheet 14 of 18	

OR_Module for burst stopper



OR_Module for burst stopper

Title: NIM		
Size: A3	Document Number: <Doc>	Rev: 3.0
Date: Monday, March 23, 2015	Sheet 14 of 18	



Title	NIM2	
Size A3	Document Number <Doc>	Rev 3.0
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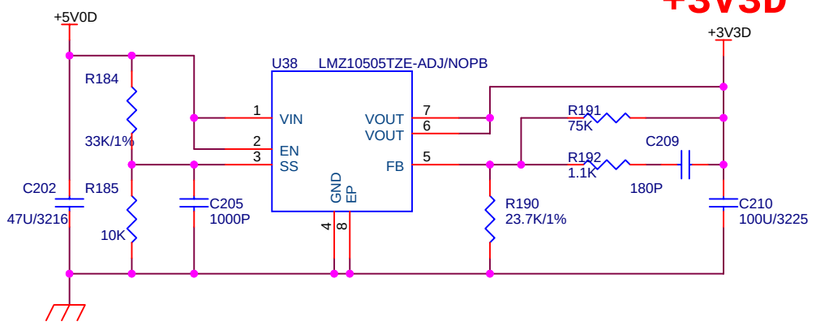
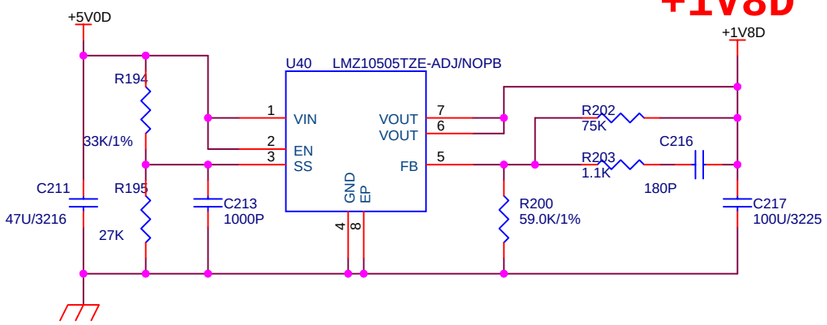
OR_Module for burst stopper

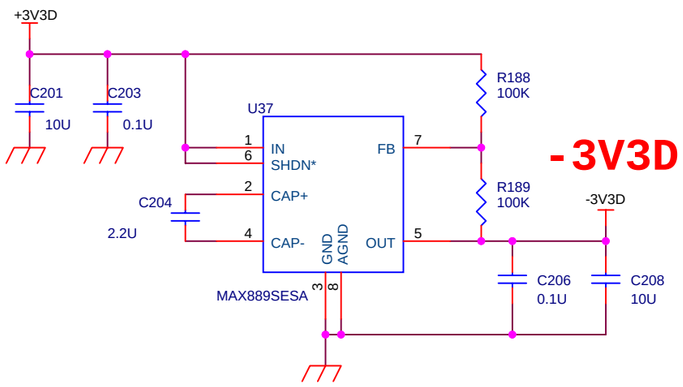
+3V3D



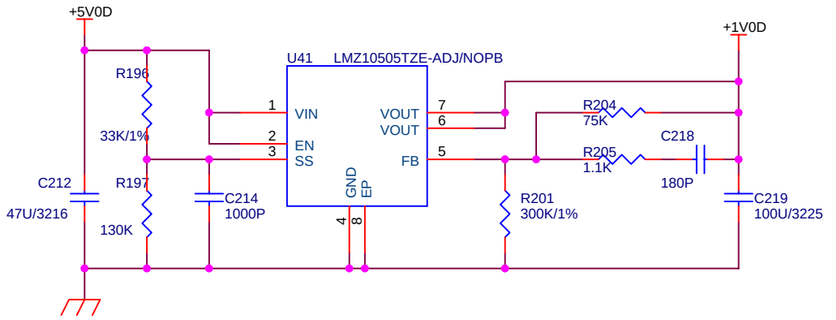
+1V8D



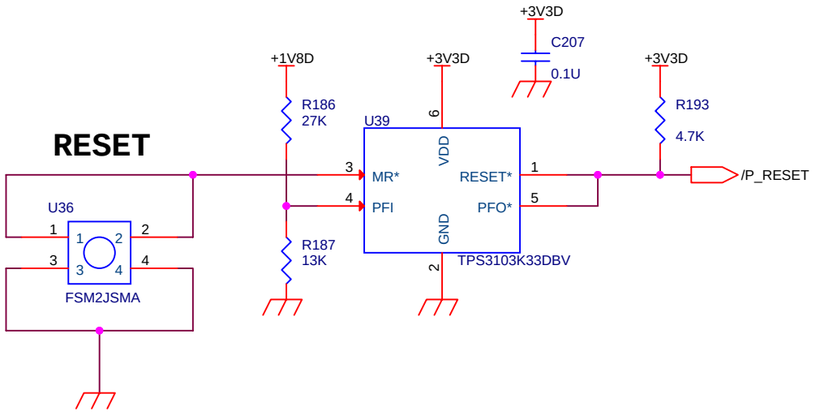
-3V3D

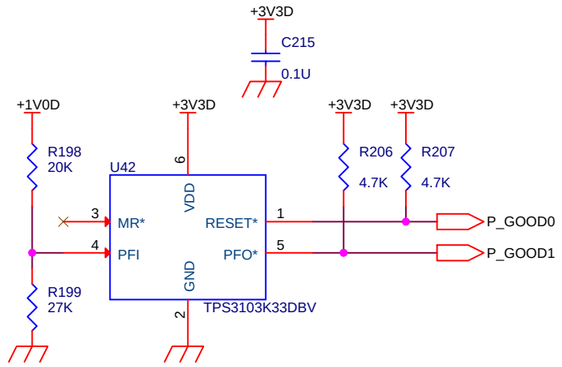


+1V0D



RESET





OR_Module for burst stopper

Title: Power		
Size: A3	Document Number	Rev: 3.0
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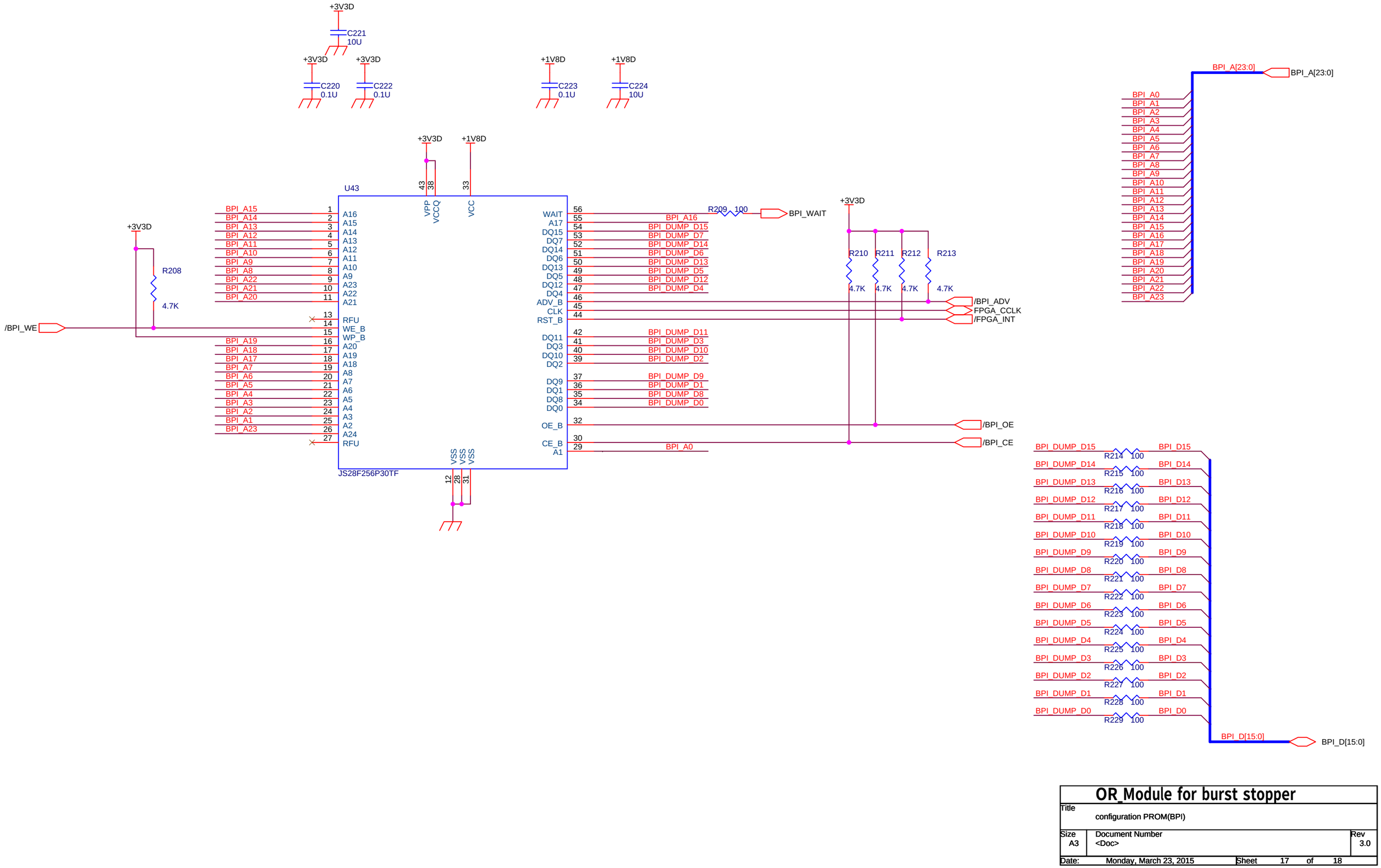

OR_Module for burst stopper

Title	configuration PROM(BPI)	
Size A3	Document Number <Doc>	Rev 3.0
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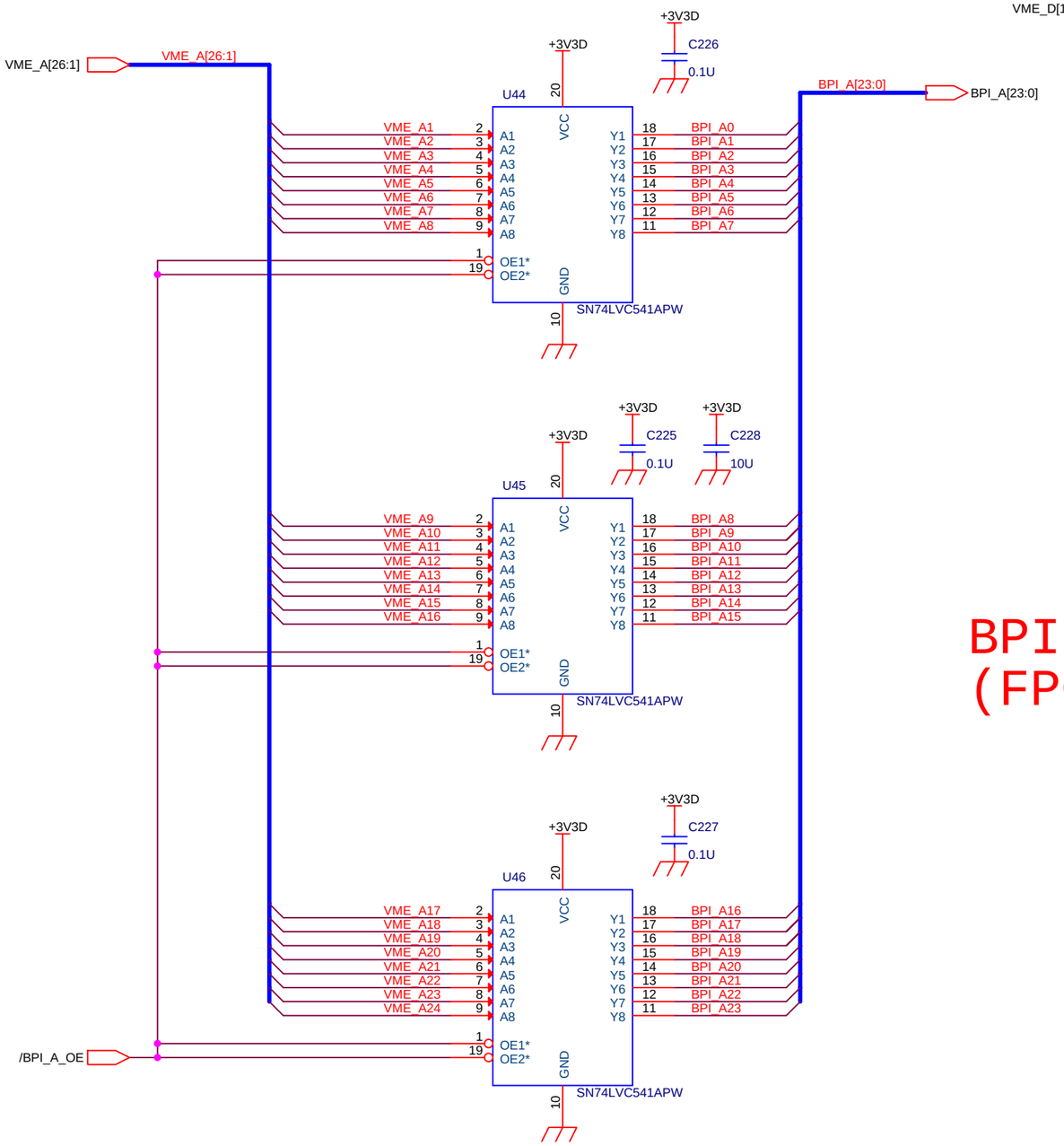
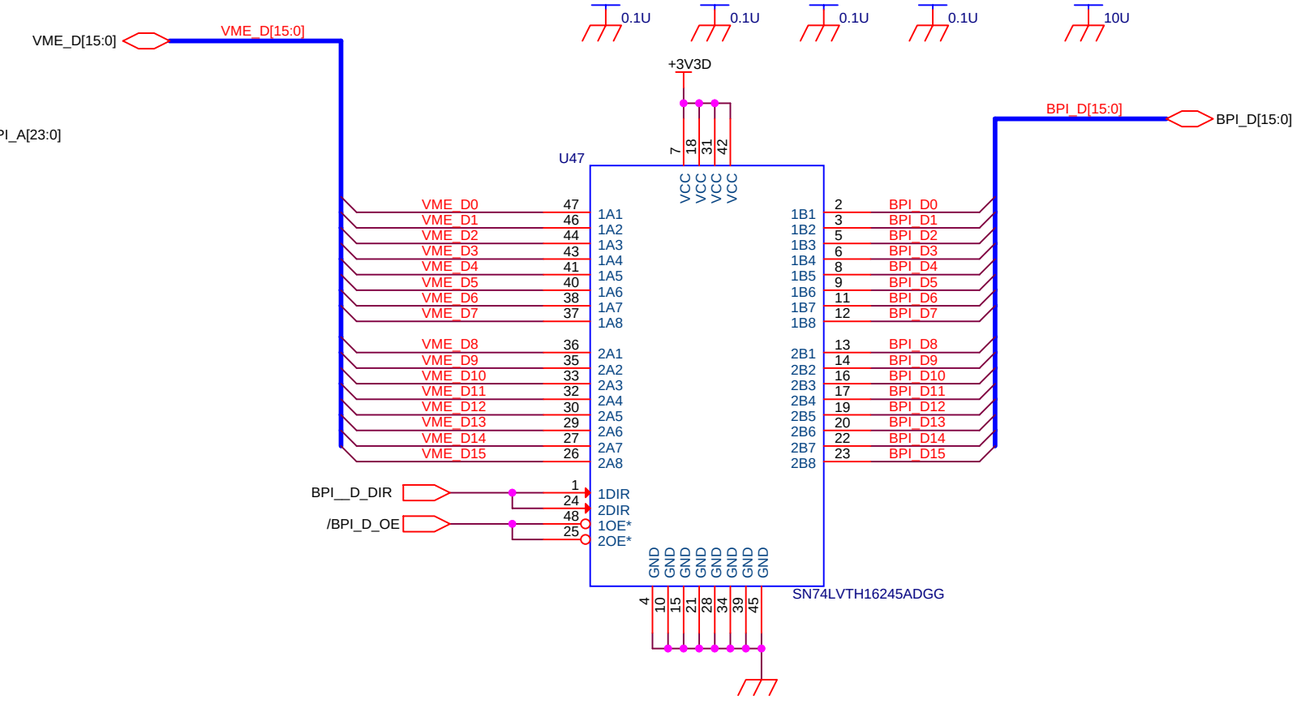
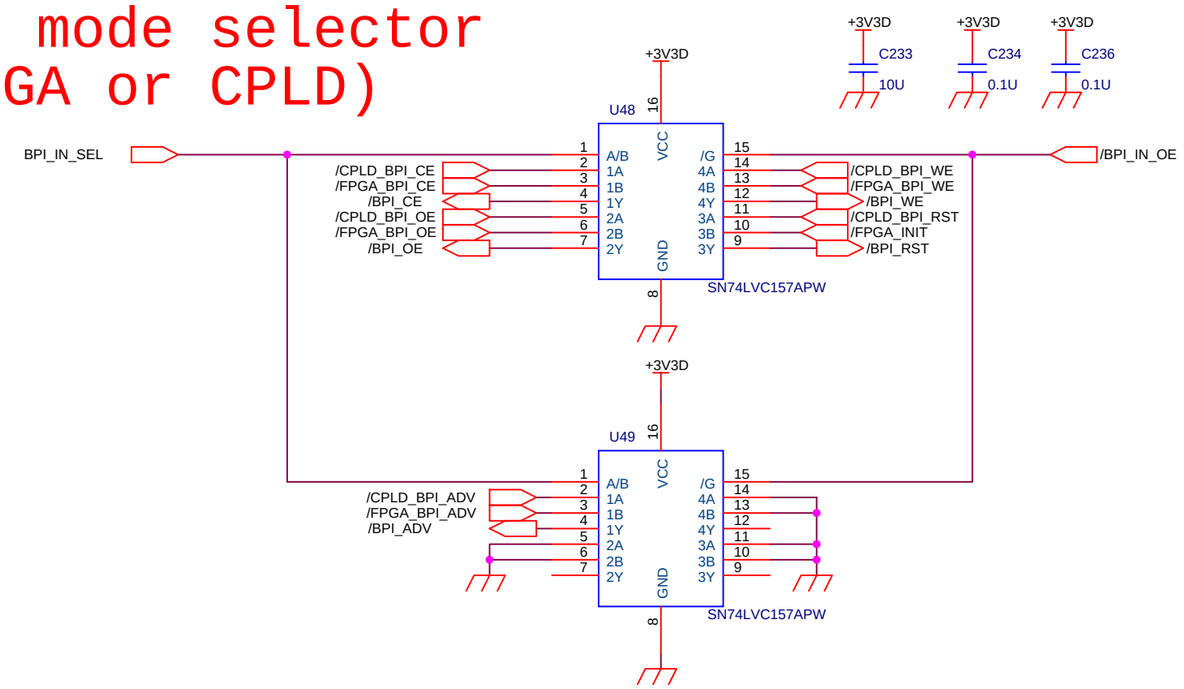
BPI address



BPI data



BPI mode selector (FPGA or CPLD)



OR_Module for burst stopper		
Title: BPI Bus, BPI mode selector		
Size: A3	Document Number: <Doc>	Rev: 3.0
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