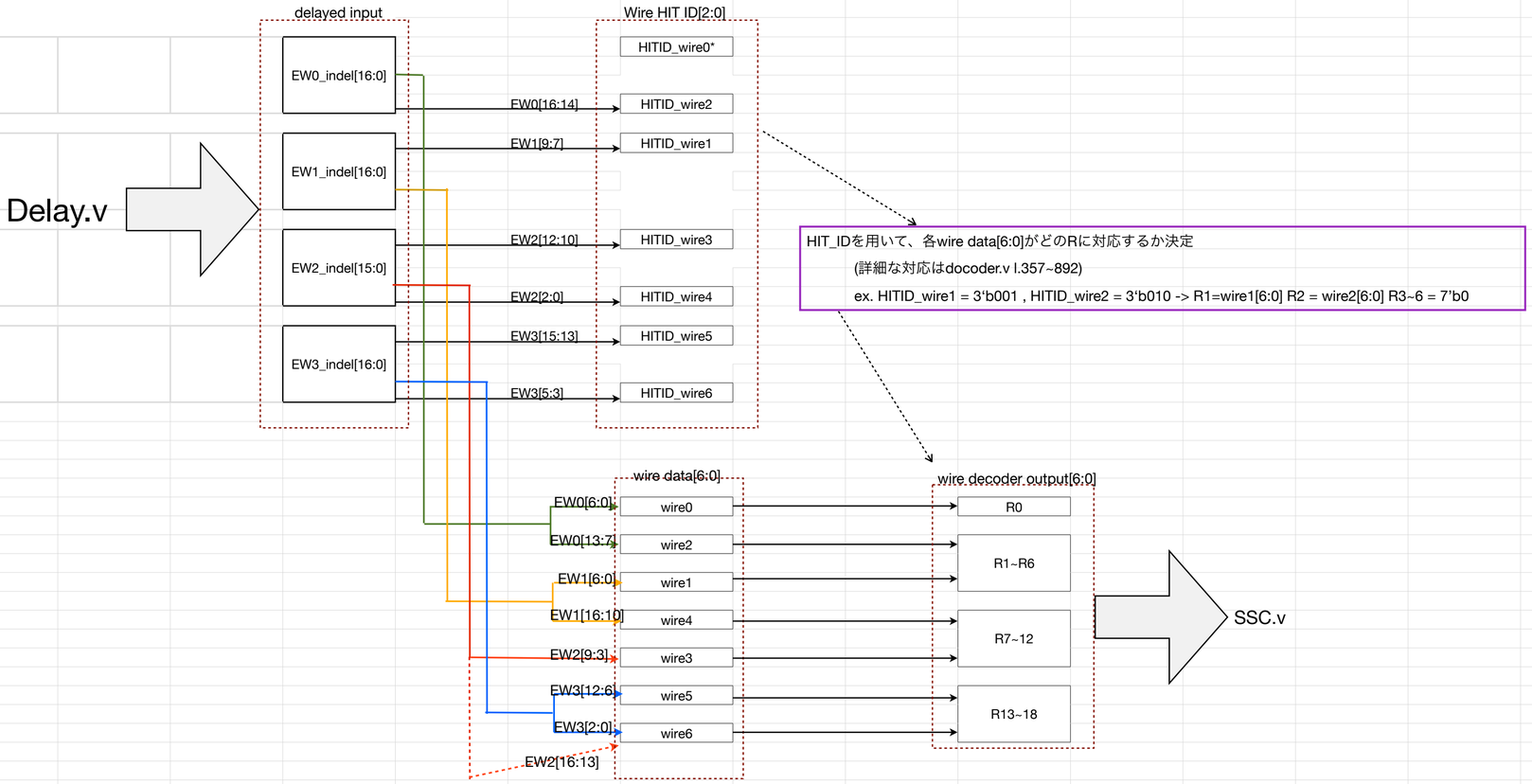
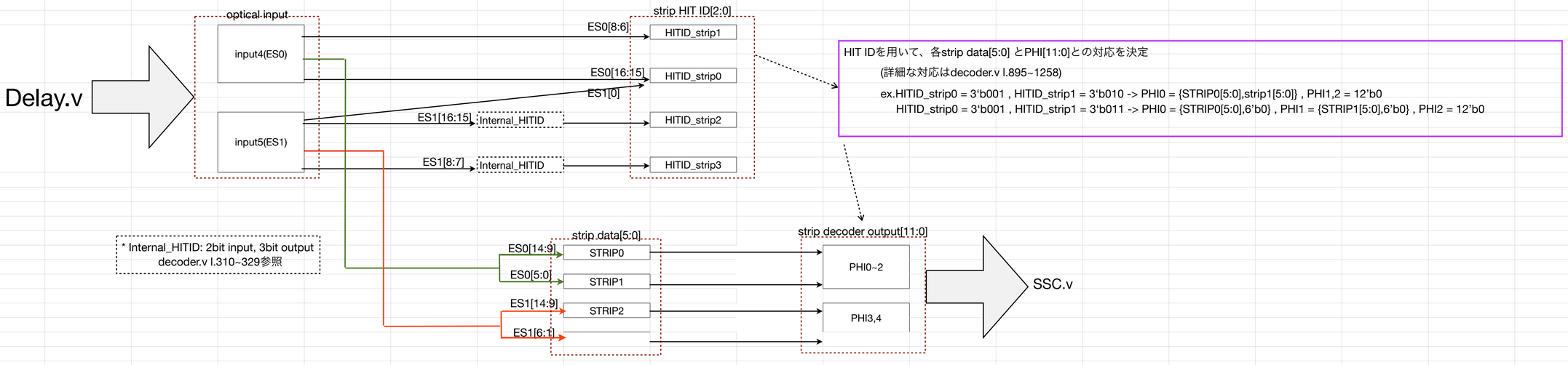
Decoder Wire Data Flow

version01: 2012/3/17



Decoder Strip Data Flow



Input/Output Data Format

Input

https://twiki.cern.ch/twiki/pub/Main/TgcDocument/HPT-SL-GLink.pdf 参照

output

R0~R18[6:0]

bit	
0	dR[0]
1	dR[1]
2	dR[2]
3	dR[3]
4	sign
5	H/L
6	pos

PHI0~3

bit	
0	dφ[0]
1	dφ[1]
2	dφ[2]
3	sign
4	H/L
5	pos
6	dφ[0]
7	dφ[1]
8	dφ[2]
9	sign
10	H/L
11	pos

hpttrg

bit	
0	EWのどれか１つでも信号が入っていたら１、それ以外は0