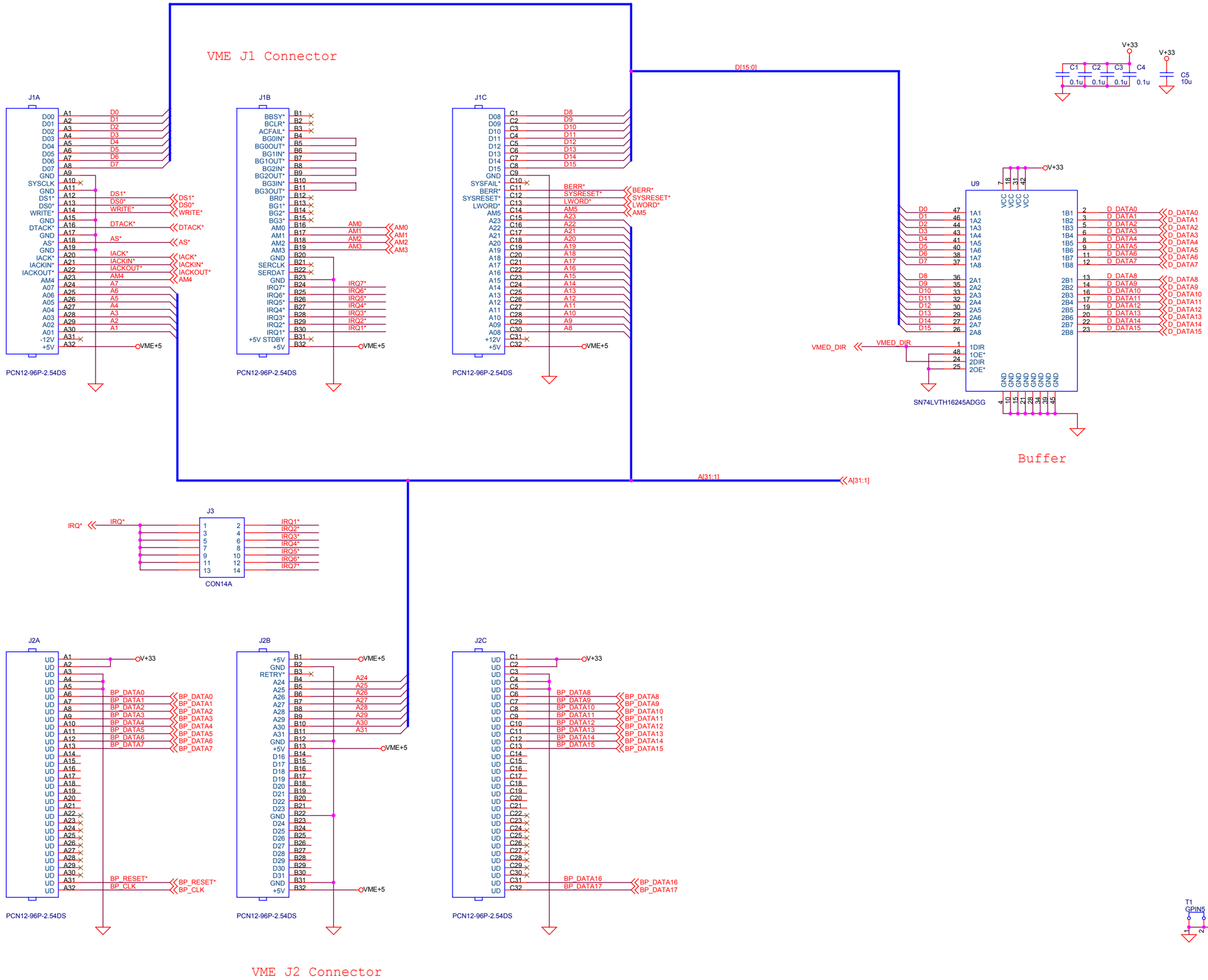
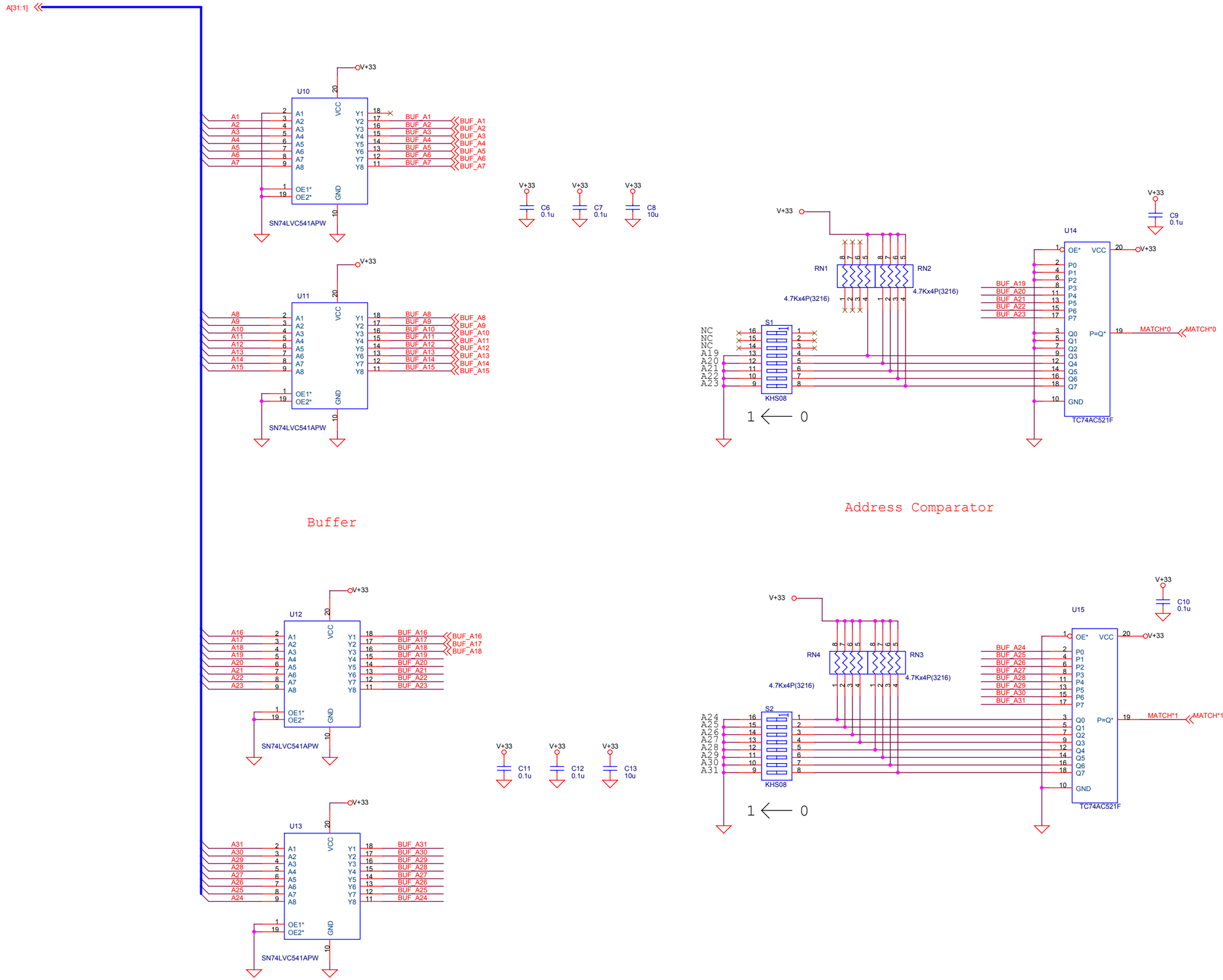
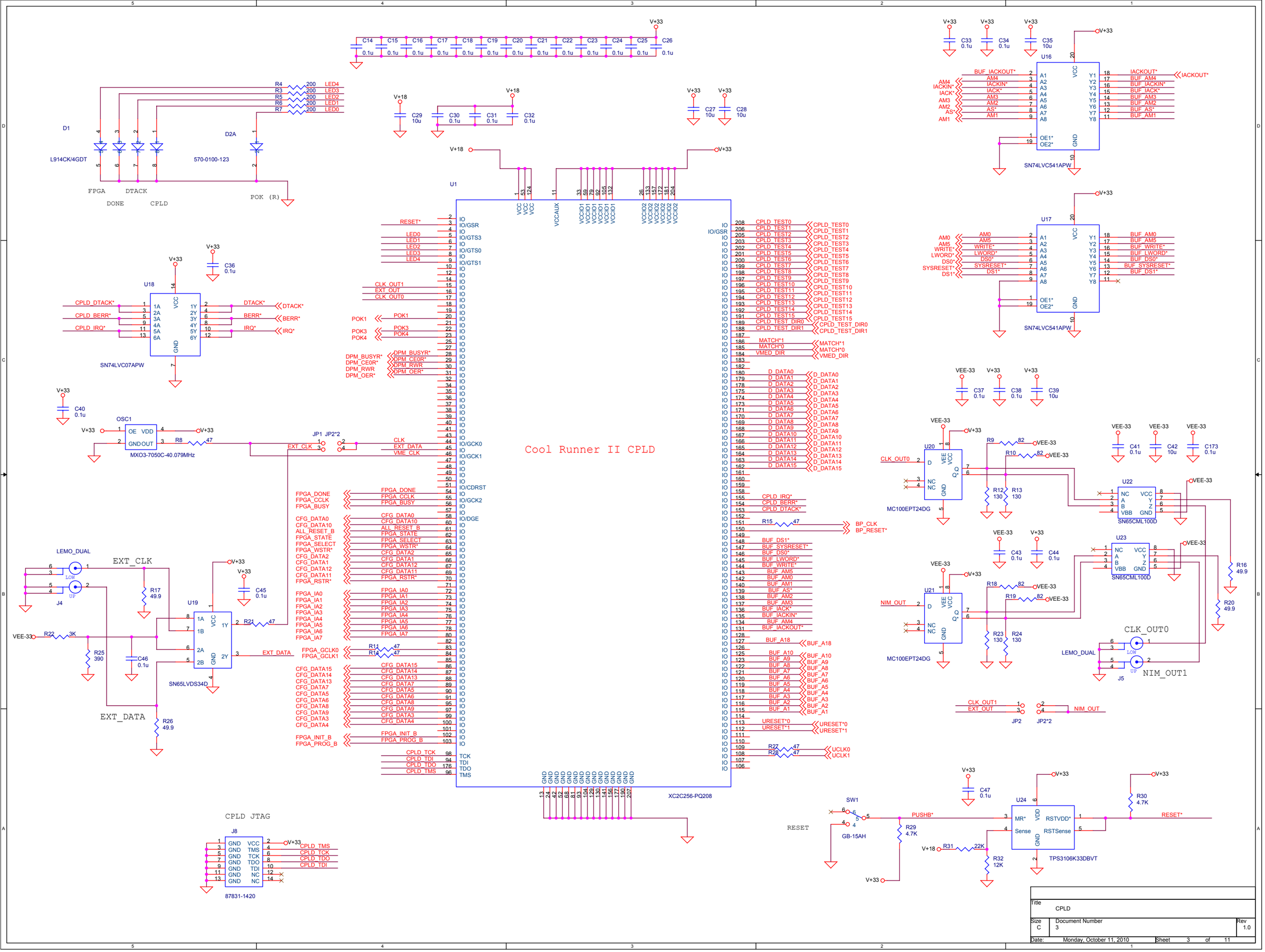
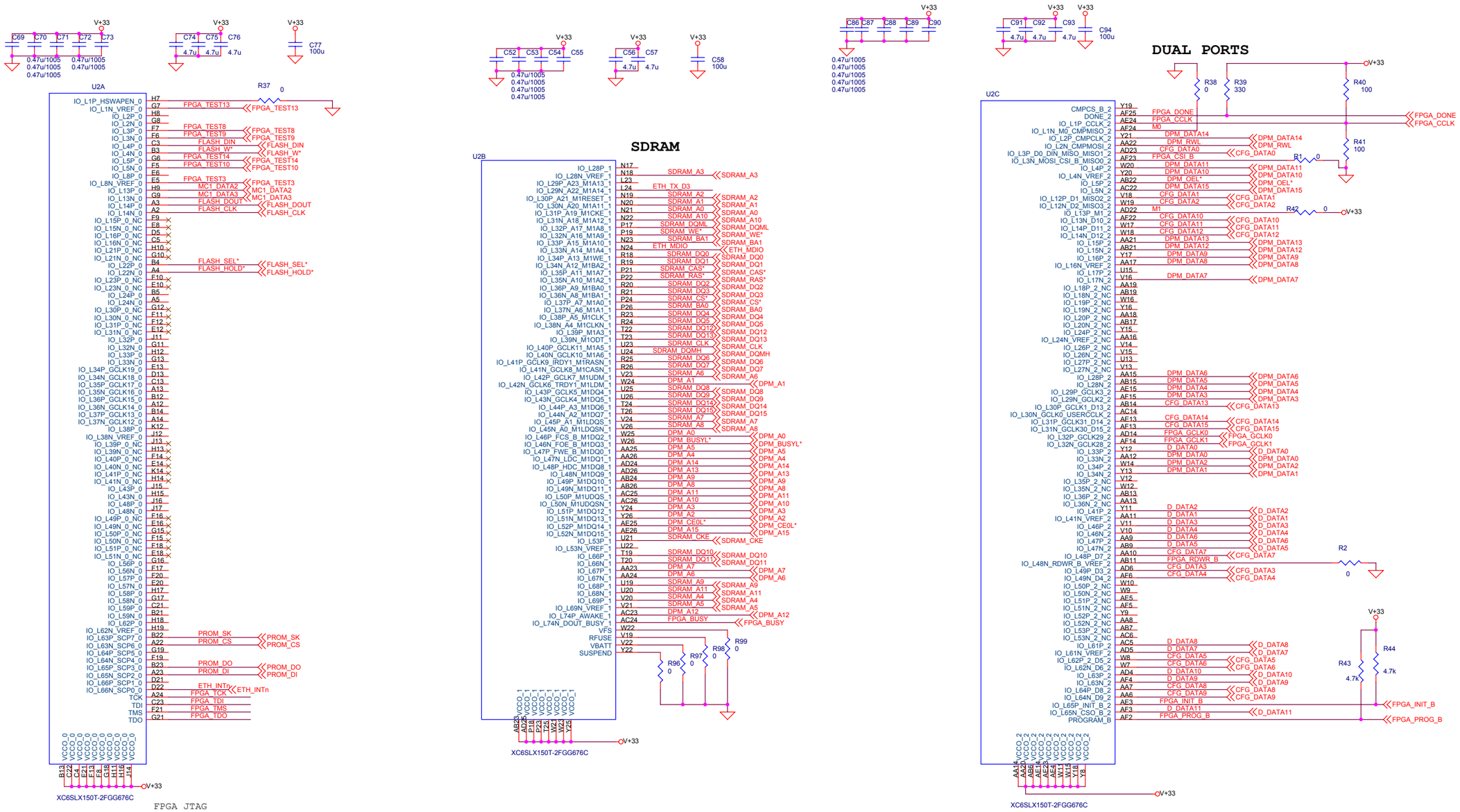


Title	VME Connector, Data Buffer
Size C	Document Number 1
Rev	1.0
Date:	Monday, October 11, 2010
Sheet	1 of 11



Title	Address Buffer, Address Comparator	
Size C	Document Number 2	Rev 1.0
Date: Monday, October 11, 2010	Sheet 2 of 11	


Cool Runner II CPLD
XC2C256-PQ208
U1
D1
L914CK/4GDT
D2A
570-0100-123
FPGA DONE
DTACK CPLD
POK (R)
U16
SN74LVC541APW
U17
SN74LVC541APW
U18
SN74LVC07APW
OSC1
MXO3-7050C-40.079MHz
JP1 JP2*2
EXT_CLK
EXT_DATA
LEMO_DUAL
J4
U19
SN65LVDS34D
U20
MC100EPT24DG
U21
MC100EPT24DG
U22
SN65CML100D
U23
SN65CML100D
CLK_OUT0
NIM_OUT1
J5
JP2
JP2*2
SW1
GB-15AH
RESET
U24
TPS3106K33DBVT
CPLD JTAG
J8
87831-1420
Title
CPLD
Size
C
Document Number
3
Rev
1.0
Date:
Monday, October 11, 2010
Sheet
3
of
11



Title	FPGA 1/2
Size A2	Document Number 4
Rev	1.0
Date:	Monday, October 11, 2010
Sheet	4 of 11

MEZA_CN1 UPPER

VMECN2

U2D

IO_L1P_3	AB5	BP_DATA2	BP_DATA2
IO_L1N_VREF_3	AC4	BP_DATA0	BP_DATA0
IO_L2P_3	AA4	BP_DATA4	BP_DATA4
IO_L2N_3	AA3	BP_DATA12	BP_DATA12
IO_L7P_3	Y6	BP_DATA6	BP_DATA6
IO_L7N_3	Y5	BP_DATA14	BP_DATA14
IO_L8P_3	AB4	BP_DATA9	BP_DATA9
IO_L8N_3	AC3	BP_DATA11	BP_DATA11
IO_L9P_3	V7	MC0_DATA40	MC0_DATA40
IO_L9N_3	V6	MC0_DATA39	MC0_DATA39
IO_L10P_3	U4	MC0_DATA30	MC0_DATA30
IO_L10N_3	U3	MC0_DATA29	MC0_DATA29
IO_L17P_3	V5	MC0_DATA38	MC0_DATA38
IO_L17N_VREF_3	W5	BP_DATA16	BP_DATA16
IO_L18P_3	U9	MC0_DATA34	MC0_DATA34
IO_L18N_3	U8	MC0_DATA33	MC0_DATA33
IO_L31P_3	U7	MC0_DATA32	MC0_DATA32
IO_L31N_VREF_3	T6	MC0_DATA24	MC0_DATA24
IO_L32P_M3DQ14_3	AB3	BP_DATA3	BP_DATA3
IO_L32N_M3DQ15_3	AB1	BP_DATA10	BP_DATA10
IO_L33P_M3DQ12_3	AD3	D_DATA13	D_DATA13
IO_L33N_M3DQ13_3	AD1	D_DATA12	D_DATA12
IO_L34P_M3UDQS_3	AC2	BP_DATA1	BP_DATA1
IO_L34N_M3UDQN_3	AC1	BP_DATA8	BP_DATA8
IO_L35P_M3DQ10_3	AE2	D_DATA15	D_DATA15
IO_L35N_M3DQ11_3	AE1	D_DATA14	D_DATA14
IO_L36P_M3DQ8_3	AA2	BP_DATA5	BP_DATA5
IO_L36N_M3DQ9_3	AA1	BP_DATA13	BP_DATA13
IO_L37P_M3DQ0_3	Y3	BP_DATA7	BP_DATA7
IO_L37N_M3DQ1_3	Y1	BP_DATA15	BP_DATA15
IO_L38P_M3DQ2_3	W2	MC0_DATA42	MC0_DATA42
IO_L38N_M3DQ3_3	W1	MC0_DATA41	MC0_DATA41
IO_L39P_M3LDQS_3	V3	MC0_DATA36	MC0_DATA36
IO_L39N_M3LDQSN_3	V1	MC0_DATA35	MC0_DATA35
IO_L40P_M3DQ6_3	U2	MC0_DATA28	MC0_DATA28
IO_L40N_M3DQ7_3	U1	MC0_DATA27	MC0_DATA27
IO_L41P_GCLK27_M3DQ4_3	T3	MC0_DATA22	MC0_DATA22
IO_L41N_GCLK26_M3DQ5_3	T1	MC0_DATA21	MC0_DATA21
IO_L42P_GCLK25_TRDY2_M3UDM_3	V4	MC0_DATA37	MC0_DATA37
IO_L42N_GCLK24_M3LDM_3	W3	BP_DATA17	BP_DATA17
IO_L43P_GCLK23_M3RASN_3	R7	MC0_DATA17	MC0_DATA17
IO_L43N_GCLK22_IRDY2_M3CASN_3	R6	MC0_DATA16	MC0_DATA16
IO_L44P_GCLK21_M3A5_3	R2	MC0_DATA12	MC0_DATA12
IO_L44N_GCLK20_M3A6_3	R1	MC0_DATA11	MC0_DATA11
IO_L45P_M3A3_3	R8	MC0_DATA18	MC0_DATA18
IO_L45N_M3ODT_3	T8	MC0_DATA25	MC0_DATA25
IO_L46P_M3CLK_3	U5	MC0_DATA31	MC0_DATA31
IO_L46N_M3CLKN_3	T4	MC0_DATA23	MC0_DATA23
IO_L47P_M3A0_3	R10	MC0_DATA20	MC0_DATA20
IO_L47N_M3A1_3	T9	MC0_DATA26	MC0_DATA26
IO_L48P_M3BA0_3	P3	MC0_DATA6	MC0_DATA6
IO_L48N_M3BA1_3	P1	MC0_DATA5	MC0_DATA5
IO_L49P_M3A7_3	N6	MC1_DATA42	MC1_DATA42
IO_L49N_M3A2_3	P6	MC0_DATA8	MC0_DATA8
IO_L50P_M3WE_3	P5	MC0_DATA7	MC0_DATA7
IO_L50N_M3BA2_3	R5	MC0_DATA15	MC0_DATA15
IO_L51P_M3A10_3	N8	MC1_DATA40	MC1_DATA40
IO_L51N_M3A4_3	N7	MC1_DATA41	MC1_DATA41
IO_L52P_M3A8_3	R4	MC0_DATA14	MC0_DATA14
IO_L52N_M3A9_3	R3	MC0_DATA13	MC0_DATA13
IO_L53P_M3CKE_3	R9	MC0_DATA19	MC0_DATA19
IO_L53N_M3A12_3	P8	MC0_DATA9	MC0_DATA9
IO_L54P_M3RESET_3	N5	MC0_DATA0	MC0_DATA0
IO_L54N_M3A11_3	N4	MC0_DATA1	MC0_DATA1
IO_L55P_M3A13_3	P10	MC0_DATA10	MC0_DATA10
IO_L55N_M3A14_3	N9	MC1_DATA39	MC1_DATA39
IO_L57P_3	M10	MC1_DATA32	MC1_DATA32
IO_L57N_VREF_3	M9	MC1_DATA33	MC1_DATA33

VCCO_3: AD2, P4, P9, T2, T7, W4, W6, Y2 — V+33

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MEZA_CN2 LOWER

U2E

IO_L58P_4	M4	MC1_DATA36	MC1_DATA36
IO_L58N_VREF_4	N3	MC0_DATA2	MC0_DATA2
IO_L59P_M4DQ14_4	N2	MC0_DATA3	MC0_DATA3
IO_L59N_M4DQ15_4	N1	MC0_DATA4	MC0_DATA4
IO_L60P_M4DQ12_4	M3	MC1_DATA37	MC1_DATA37
IO_L60N_M4DQ13_4	M1	MC1_DATA38	MC1_DATA38
IO_L61P_M4UDQS_4	L2	MC1_DATA30	MC1_DATA30
IO_L61N_M4UDQSN_4	L1	MC1_DATA31	MC1_DATA31
IO_L62P_M4DQ10_4	K3	MC1_DATA21	MC1_DATA21
IO_L62N_M4DQ11_4	K1	MC1_DATA22	MC1_DATA22
IO_L63P_M4DQ8_4	J2	MC1_DATA13	MC1_DATA13
IO_L63N_M4DQ9_4	J1	MC1_DATA14	MC1_DATA14
IO_L64P_M4DQ0_4	H3	MC1_DATA6	MC1_DATA6
IO_L64N_M4DQ1_4	H1	MC1_DATA7	MC1_DATA7
IO_L65P_M4DQ2_4	G2	MC1_DATA0	MC1_DATA0
IO_L65N_M4DQ3_4	G1	MC1_DATA1	MC1_DATA1
IO_L66P_M4LDQS_4	F3	FPGA_TEST11	FPGA_TEST11
IO_L66N_M4LDQSNN_4	F1	FPGA_TEST12	FPGA_TEST12
IO_L67P_M4DQ6_4	E2	FPGA_TEST6	FPGA_TEST6
IO_L67N_M4DQ7_4	E1	FPGA_TEST7	FPGA_TEST7
IO_L68P_M4DQ4_4	D3	FPGA_TEST1	FPGA_TEST1
IO_L68N_M4DQ5_4	D1	FPGA_TEST2	FPGA_TEST2
IO_L69P_M4UDM_4	J4	MC1_DATA11	MC1_DATA11
IO_L69N_M4LDM_4	J3	MC1_DATA12	MC1_DATA12
IO_L70P_M4RASN_4	L9	MC1_DATA24	MC1_DATA24
IO_L70N_M4CASN_4	L8	MC1_DATA25	MC1_DATA25
IO_L71P_M4A5_4	L4	MC1_DATA28	MC1_DATA28
IO_L71N_M4A6_4	L3	MC1_DATA29	MC1_DATA29
IO_L72P_M4A3_4	M8	MC1_DATA34	MC1_DATA34
IO_L72N_M4ODT_4	M6	MC1_DATA35	MC1_DATA35
IO_L73P_M4CLK_4	K5	MC1_DATA20	MC1_DATA20
IO_L73N_M4CLKN_4	J5	MC1_DATA10	MC1_DATA10
IO_L74P_M4A0_4	L7	MC1_DATA26	MC1_DATA26
IO_L74N_M4A1_4	L6	MC1_DATA27	MC1_DATA27
IO_L75P_M4BA0_4	B2	CONSOLE_TX	CONSOLE_TX
IO_L75N_MABA1_4	B1	CONSOLE_RX	CONSOLE_RX
IO_L76P_M4A7_4	L10	MC1_DATA23	MC1_DATA23
IO_L76N_M4A2_4	K10	MC1_DATA15	MC1_DATA15
IO_L77P_M4WE_4	G4	FPGA_TEST15	FPGA_TEST15
IO_L77N_M4BA2_4	G3	FPGA_TEST_DIR1	FPGA_TEST_DIR1
IO_L78P_M4A10_4	J9	MC1_DATA8	MC1_DATA8
IO_L78N_M4A4_4	J7	MC1_DATA9	MC1_DATA9
IO_L79P_M4A8_4	C2	FPGA_TEST_DIR0	FPGA_TEST_DIR0
IO_L79N_M4A9_4	C1	FPGA_TEST0	FPGA_TEST0
IO_L80P_M4CKE_4	K9	MC1_DATA16	MC1_DATA16
IO_L80N_M4A12_4	K8	MC1_DATA17	MC1_DATA17
IO_L81P_M4RESET_4	E4	FPGA_TEST4	FPGA_TEST4
IO_L81N_M4A11_4	E3	FPGA_TEST5	FPGA_TEST5
IO_L82P_M4A13_4	K7	MC1_DATA18	MC1_DATA18
IO_L82N_M4A14_4	K6	MC1_DATA19	MC1_DATA19
IO_L83P_4	H6	MC1_DATA4	MC1_DATA4
IO_L83N_VREF_4	H5	MC1_DATA5	MC1_DATA5

VCCO_4: D2, E4, H2, J6, K4, M2, M7 — V+33

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FPGA TEST

ETH CPLD

U2F

IO_L1P_A25_5	H20	FPGA_STATE	FPGA_STATE
IO_L1N_A24_VREF_5	G20	ALL_RESET_B	ALL_RESET_B
IO_L2P_M5A13_5	B24	ETH_COL	ETH_COL
IO_L2N_M5A14_5	A25	ETH_RSTn	ETH_RSTn
IO_L3P_M5RESET_5	K18		
IO_L3N_M5A11_5	K19	FPGA_IA2	FPGA_IA2
IO_L4P_M5CKE_5	D23	LED_ACT	LED_ACT
IO_L4N_M5A12_5	C24	ETH_RX_ER	ETH_RX_ER
IO_L5P_M5A8_5	H21	FPGA_SELECT	FPGA_SELECT
IO_L5N_M5A9_5	H22	FPGA_WSTR*	FPGA_WSTR*
IO_L6P_M5A10_5	F22	LED_100M	LED_100M
IO_L6N_M5A4_5	G23	LED_FULL	LED_FULL
IO_L7P_M5WE_5	J20	FPGA_RSTR*	FPGA_RSTR*
IO_L7N_M5BA2_5	J22	FPGA_IA0	FPGA_IA0
IO_L8P_M5A7_5	E23	LED_10M	LED_10M
IO_L8N_M5A2_5	E24	ETH_RX_D4	
IO_L9P_M5BA0_5	L19	FPGA_IA6	FPGA_IA6
IO_L9N_M5BA1_5	K20	FPGA_IA3	FPGA_IA3
IO_L10P_M5A0_5	C25	ETH_RX_DV	ETH_RX_DV
IO_L10N_M5A1_5	C26	ETH_RX_D7	
IO_L11P_M5CLK_5	B25	ETH_CRS	ETH_CRS
IO_L11N_M5CLKN_5	B26		
IO_L12P_M5A3_5	K21	FPGA_IA4	FPGA_IA4
IO_L12N_M5ODT_5	K22	FPGA_IA5	FPGA_IA5
IO_L13P_M5A5_5	M18		
IO_L13N_M5A6_5	M19		
IO_L14P_M5RASN_5	F23	LED_1000M	LED_1000M
IO_L14N_M5CASN_5	G24		
IO_L15P_M5UDM_5	J23	FPGA_IA1	FPGA_IA1
IO_L15N_M5LDM_5	J24	ETH_TX_EN	ETH_TX_EN
IO_L16P_M5DQ4_5	F25	ETH_RX_D3	
IO_L16N_M5DQ5_5	E26	ETH_RX_D2	
IO_L17P_M5DQ6_5	D24	ETH_RX_D6	
IO_L17N_M5DQ7_5	D26	ETH_RX_D5	
IO_L18P_M5LDQS_5	F24	ETH_RX_D1	
IO_L18N_M5LDQSN_5	F26	ETH_RX_D0	
IO_L19P_M5DQ2_5	H24	ETH_TX_CLK	ETH_TX_CLK
IO_L19N_M5DQ3_5	H26	ETH_TX_ER	ETH_TX_ER
IO_L20P_M5DQ0_5	G25	ETH_RX_CLK	ETH_RX_CLK
IO_L20N_M5DQ1_5	G26		
IO_L21P_M5DQ8_5	K24	ETH_TX_D5	
IO_L21N_M5DQ9_5	K26	ETH_TX_D4	
IO_L22P_M5DQ10_5	J25	ETH_TX_D7	
IO_L22N_M5DQ11_5	J26	ETH_TX_D6	
IO_L23P_M5UDQS_5	M24	ETH_TX_D0	
IO_L23N_M5UDQSN_5	M26	ETH_GTXCLK	ETH_GTXCLK
IO_L24P_M5DQ12_5	L25	ETH_TX_D2	
IO_L24N_M5DQ13_5	L26	ETH_TX_D1	
IO_L25P_M5DQ14_5	N25	ETH_MDC	ETH_MDC
IO_L25N_M5DQ15_5	N26	ETH_MACCLK	ETH_MACCLK
IO_L26P_5	M21		
IO_L26N_VREF_5	M23		
IO_L27P_5	L20	FPGA_IA7	FPGA_IA7
IO_L27N_5	L21		

VCCO_5: D25, G22, H25, J21, K23, M20, M25 — V+33

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ETH_TX_D3 — ETH_TX_D[7:0]

ETH_TX_D1, ETH_TX_D2, ETH_TX_D5, ETH_TX_D6, ETH_TX_D0, ETH_TX_D4, ETH_RX_D6, ETH_RX_D7, ETH_TX_D7, ETH_RX_D3, ETH_RX_D4, ETH_RX_D5, ETH_RX_D0, ETH_RX_D1, ETH_RX_D2 — ETH_RX_D[7:0]

C78 0.47u/1005, C79 4.7u/1005, C80 4.7u/1005, C81 4.7u/1005, C82 4.7u/1005 — V+33

C83 4.7u, C84 4.7u — V+33

C85 100u — V+33

C150 0.47u/1005, C151 4.7u/1005, C152 4.7u/1005 — V+33

C153 4.7u, C154 4.7u — V+33

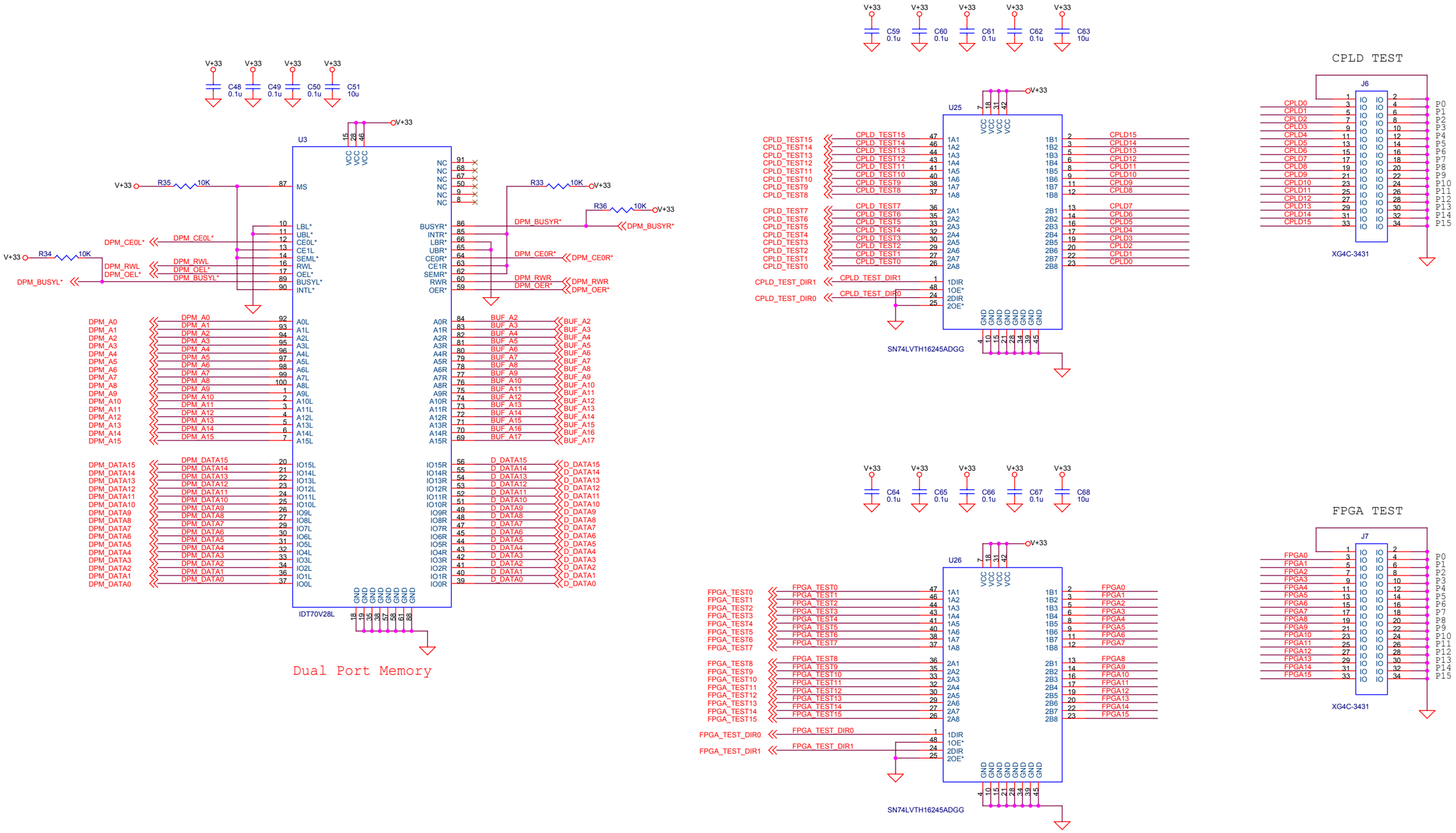
C155 100u — V+33

C156 0.47u/1005, C157 4.7u/1005, C158 4.7u/1005, C159 4.7u/1005 — V+33

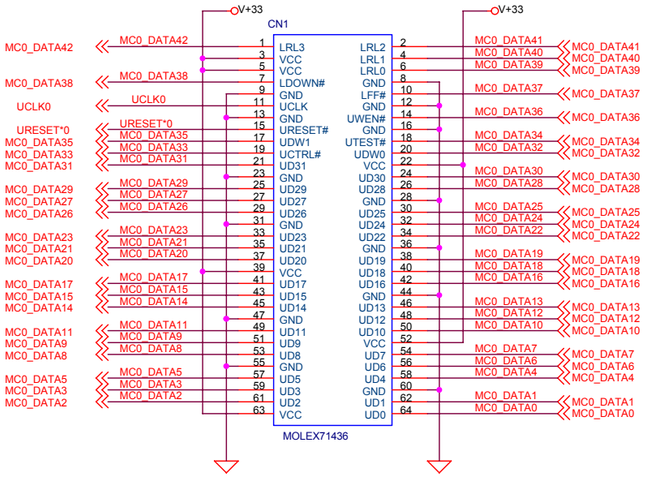
C160 4.7u, C161 4.7u — V+33

C162 100u — V+33

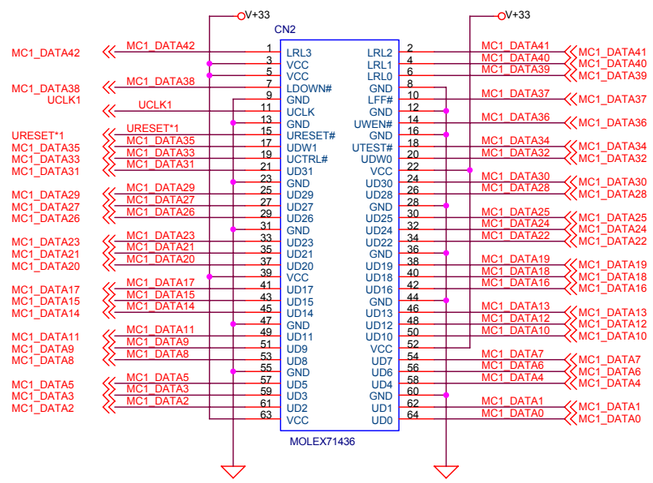
Title	FPGA 2/2	
Size A3	Document Number 5	Rev 1.0
Date: Monday, October 11, 2010	Sheet 5 of 11	



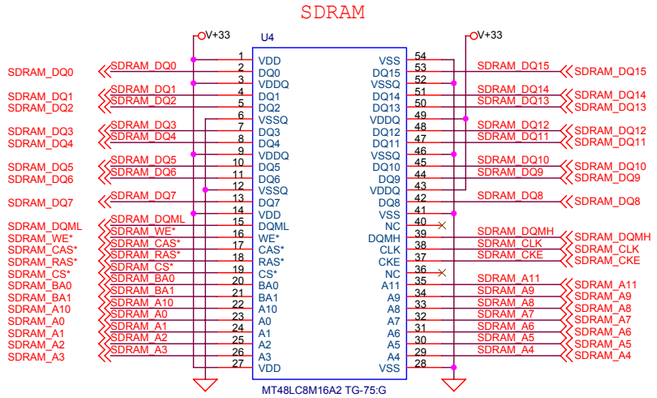
Title	Dual Port Memory, Test Pin
Size C	Document Number 6
Rev	1.0
Date:	Monday, October 11, 2010
Sheet	6 of 11

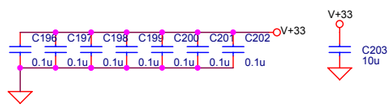


Mezzanine Card Connector

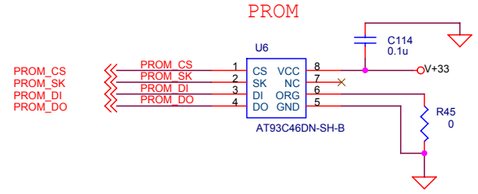


SDRAM

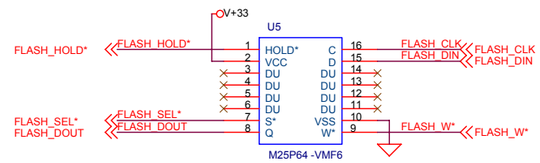


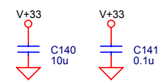


PROM

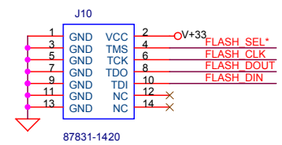


Flash Memory

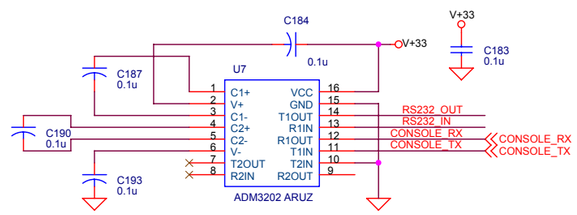




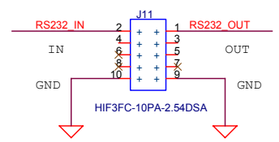
SPI Flash



RS232 DRV/REC



RS232



Title	Mezzanine Card, SDRAM, PROM, Flash, RS232	
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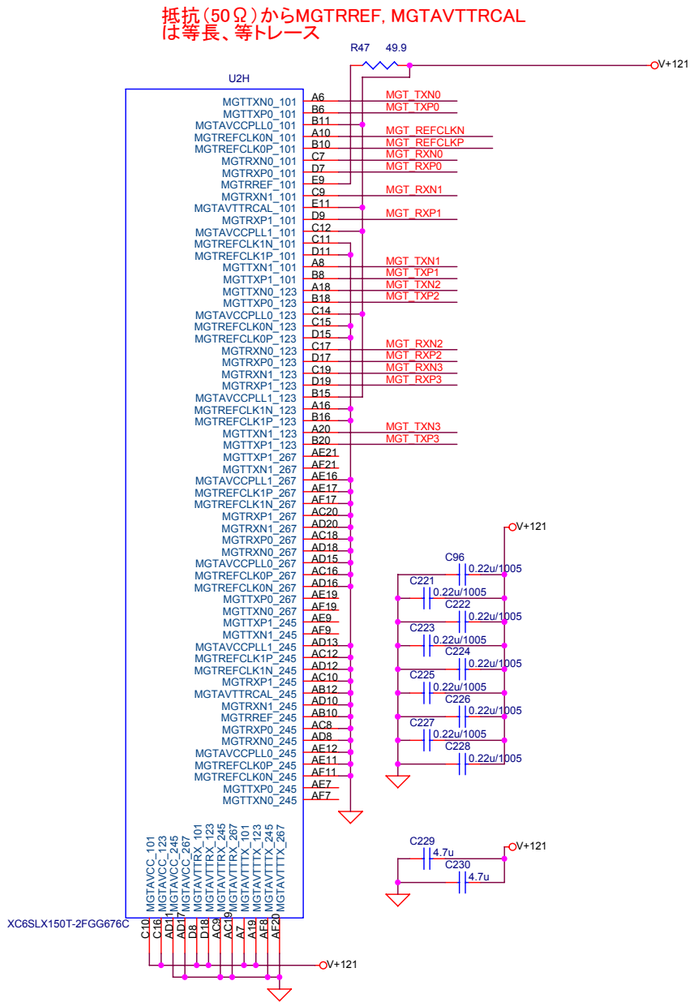
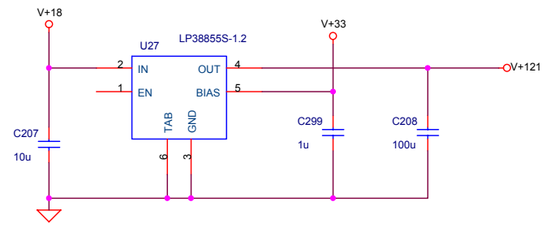
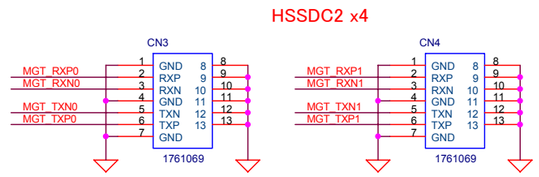
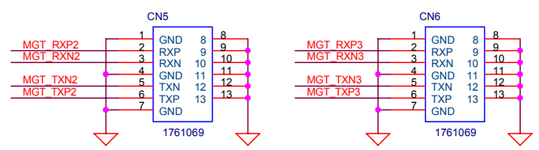
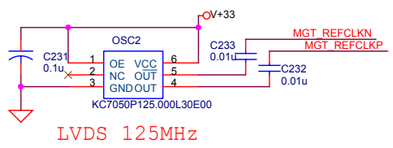






MGTの差動ペアは等長、差動100Ω





LVDS 125MHz

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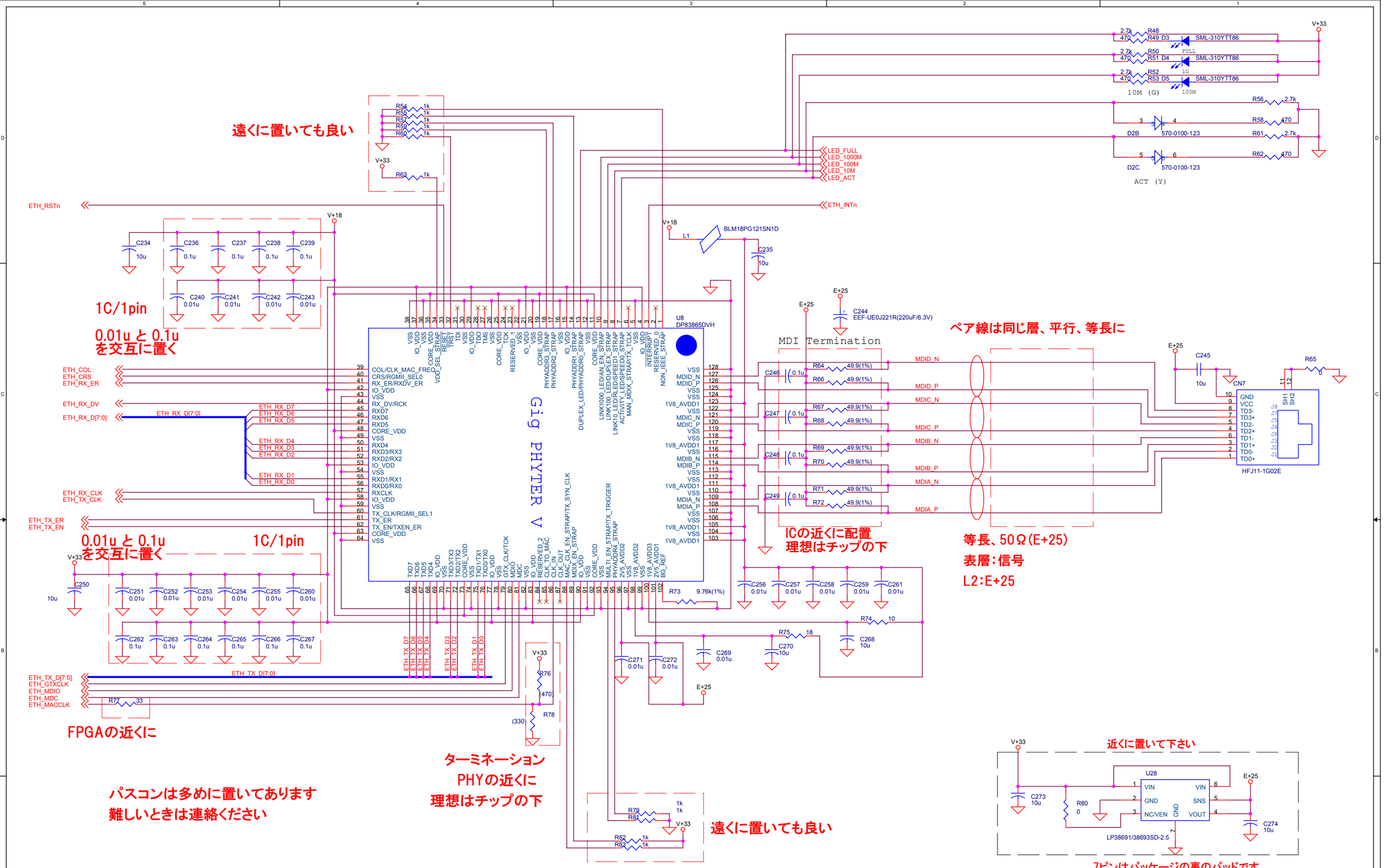

近くに置いて下さい

7ピンはパッケージの裏のパッドです。
また、ヒートシンクを兼ねているのでビアでGNDに落としてください
E+25VはEthernetのアナログ用電源です

Title	Gigabit Ethernet	
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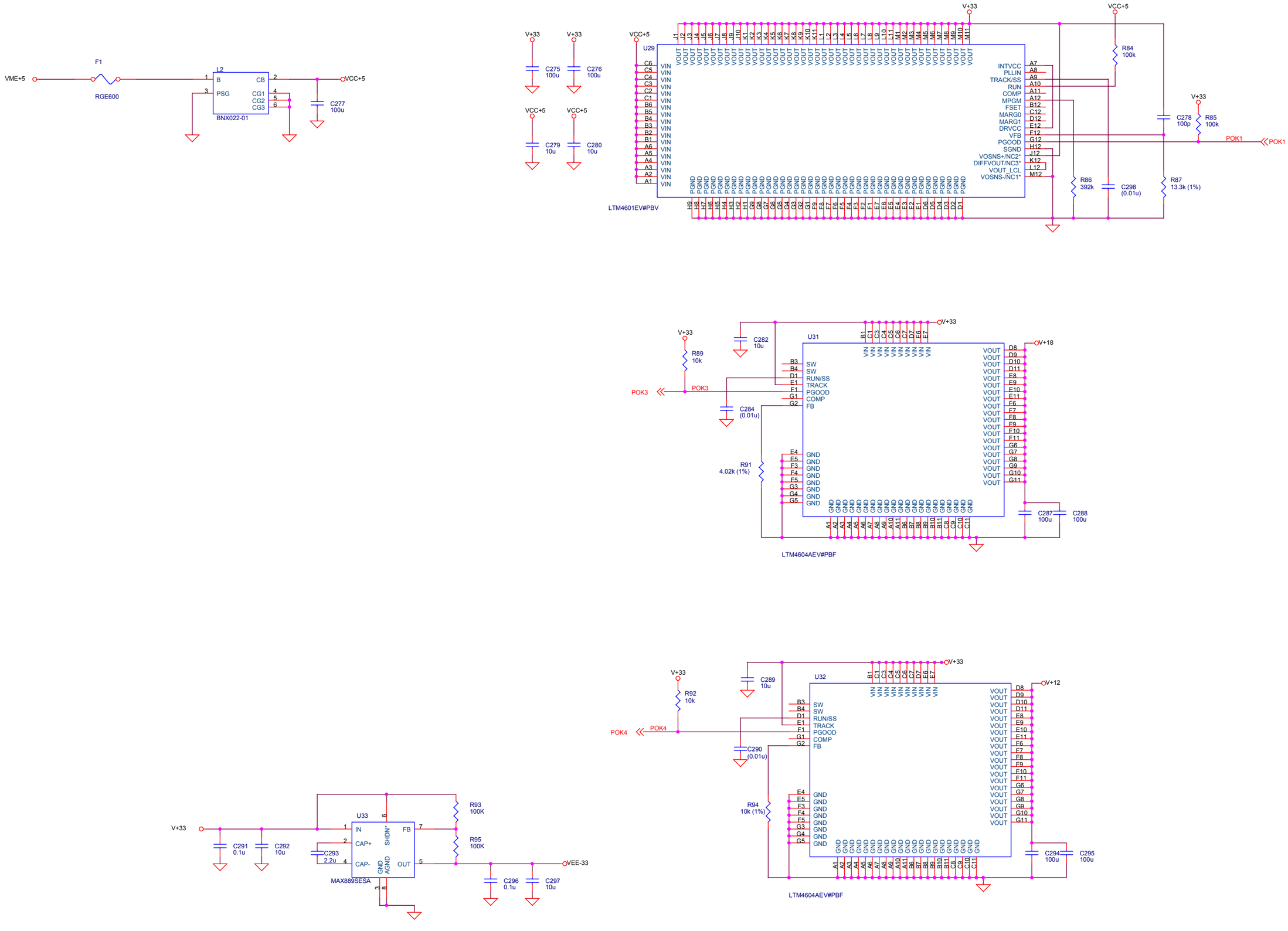

Title	Power
Size C	Document Number 10
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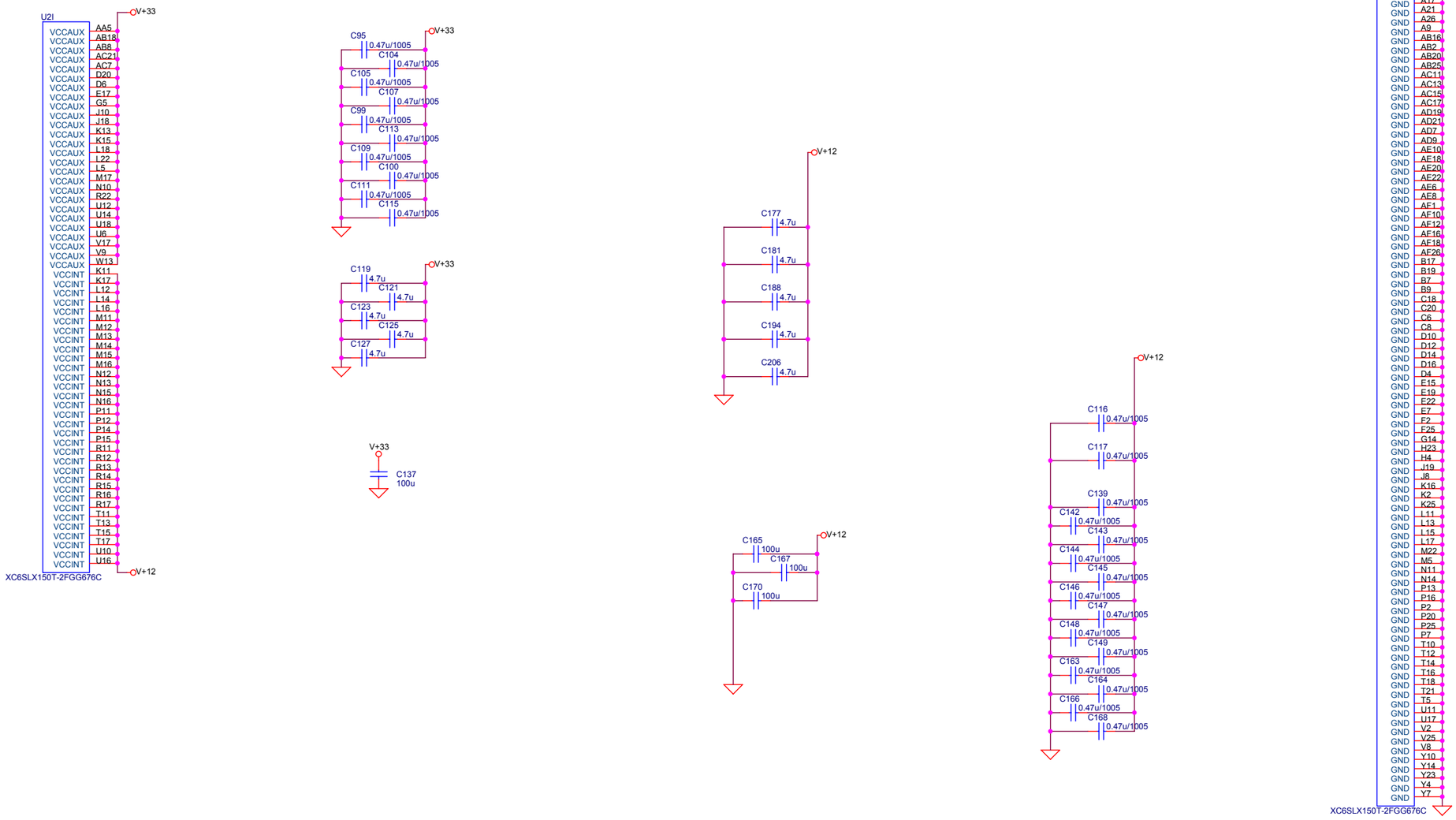

Title	GND, VCC	
Size C	Document Number 11	Rev 1.0
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